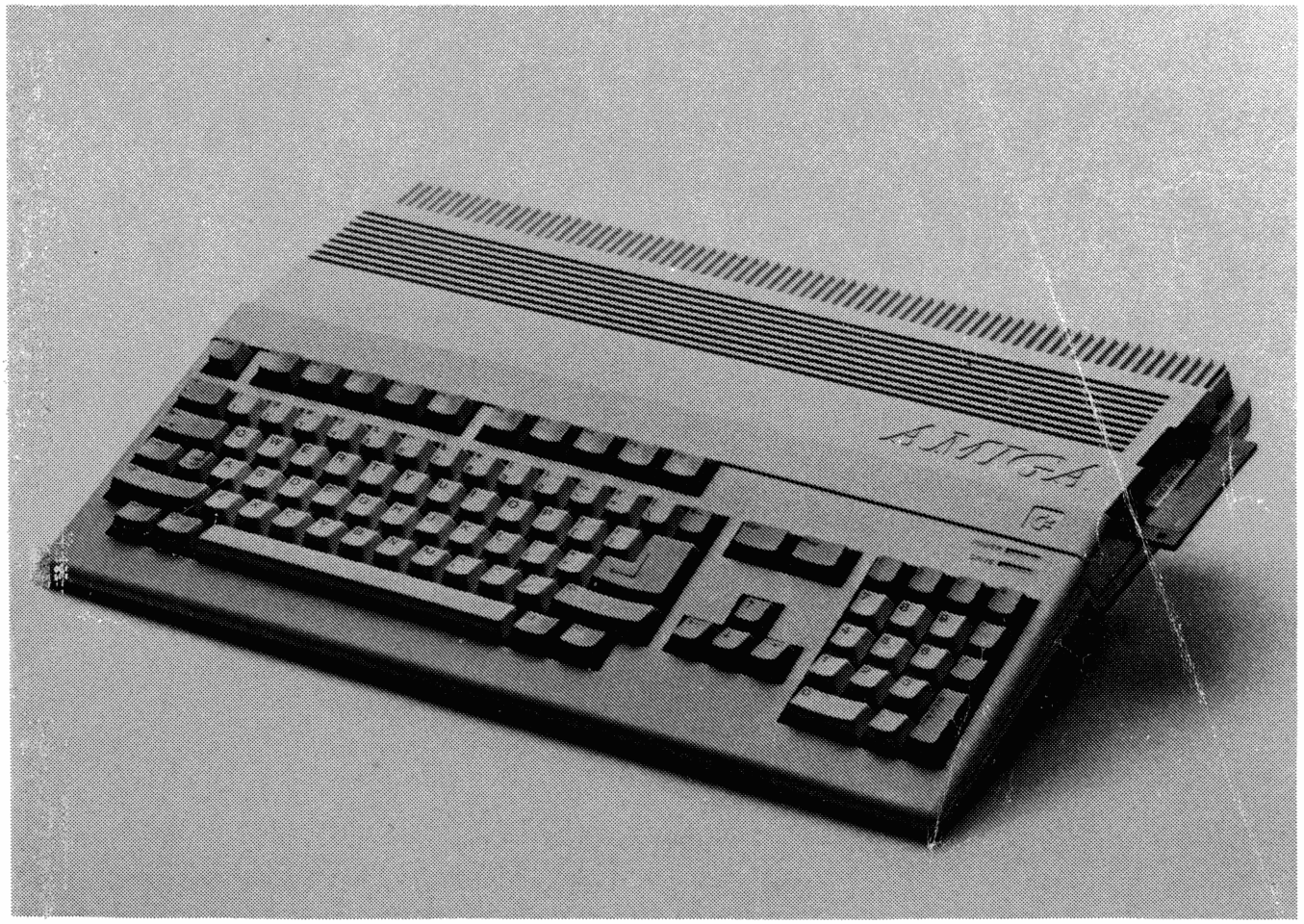
# Technical Manual

# COMMODORE AMIGA 500




Commodore

# *SERVICE MANUAL*

# A500

**JUNE, 1987** **PN-314981-01**

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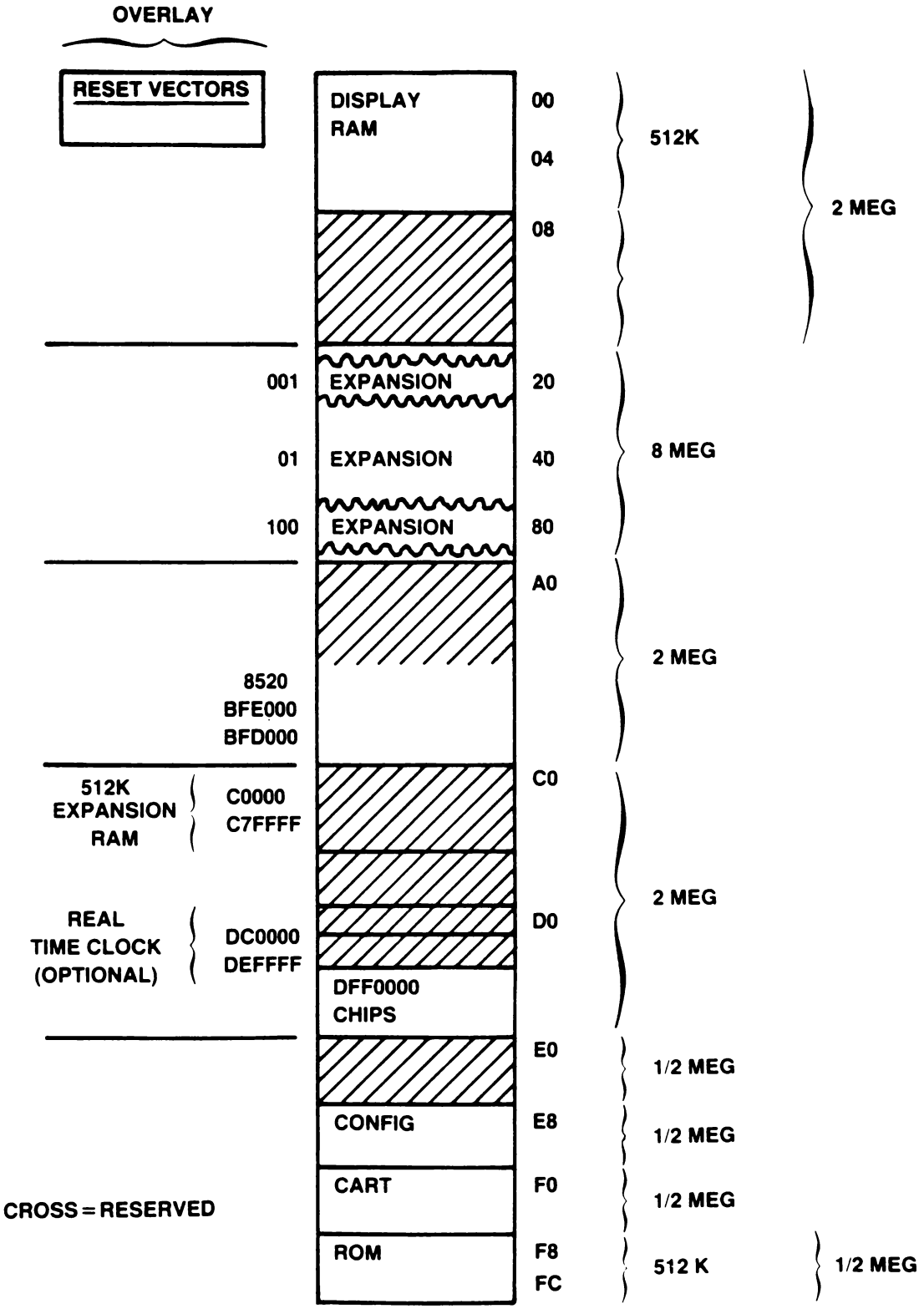
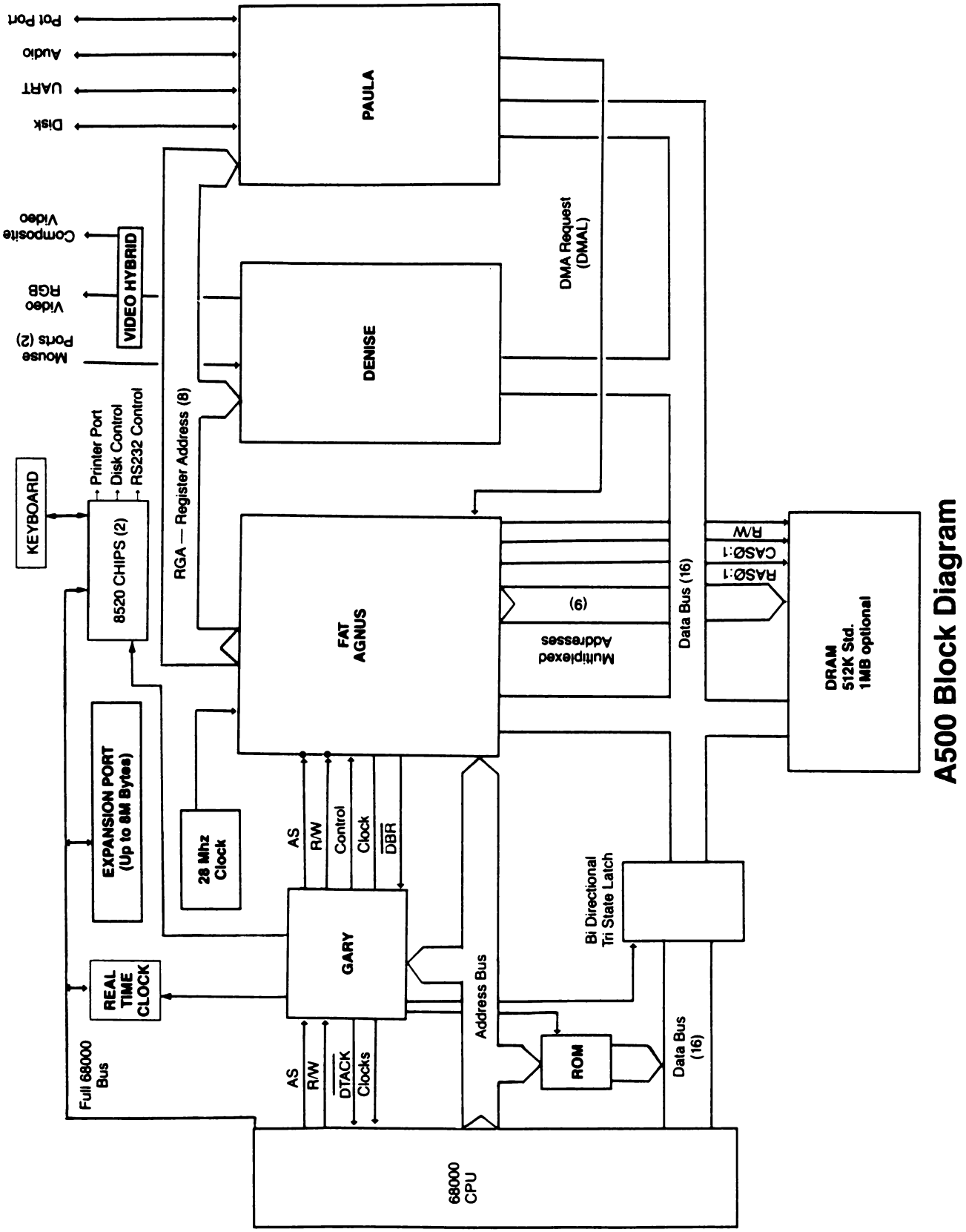
# TABLE OF CONTENTS

# Amiga Specifications

| | |
|---|---|
| **Central Processor** | Motorola MC68000 |
| **Memory** | 512K bytes RAM expandable to 1M |
| **Disks** | 3-1/2 inch double-sided double-density microdisks with 880K bytes formatted storage capacity per disk |
| **Mouse** | Mechanical, .13 mm/count (200 counts per inch) |
| **Interfaces** | RS-232 serial interface<br>Centronics®-compatible parallel interface<br>External disk interface<br>Mouse/Game controller interface<br>Additional game controller interface<br>Keyboard interface<br>Two audio outputs for stereo sound<br>Memory cartridge interface<br>Expansion interface |
| **Supported Monitors** | Analog RGB, digital RGB, monochrome (composite video), and standard televisions |
| **Power Requirements** | 99 to 121 volts AC 54 to 66 Hz |
| **Temperature Requirements** | For operation:<br>5 to 40 degrees Centigrade<br>(41 to 104 degrees Fahrenheit)<br>For storage:<br>-40 to 60 degrees Centigrade<br>(-40 to 140 degrees Fahrenheit) |
| **Humidity Requirements** | 20% to 90% relative humidity,<br>non-condensing |

# Amiga 500 Memory Map






A500 Block Diagram

# Theory of Operation

The AMIGA computer is a high-performance system with advanced graphics and audio features. The principal hardware features consist of the 68000 microprocessor which runs at 7.2 MHz, 512K RAM, expandable to 1MB, and configurable to 8MB, 2 parallel I/O chips, one control chip (GARY) and 3 custom VLSI chips that provide the unique capabilities for animation, graphics and sound.

## 68000 Microprocessor

The 68000 is the CPU of the system. All other resources are under software control via control data issued from it. All 3 custom chips have control registers that are written by the 68000.

The 68000 communicates with the rest of the computer via its address bus, data bus and control lines. Notice that in the block diagram the 3 custom chips do not reside directly on the 68000 buses. When the 68000 starts a bus cycle that is intended for the custom chips or the display RAM, the bus control chip detects whether or not the display RAM buses are available. The control chip will not assert the acknowledge signal (/DTACK) back to the 68000 until the display RAM buses are available. Once the 68000 receives /DTACK it completes the bus cycle. Connecting the display RAM buses to the 68000 buses is discussed further in the section on bus control. Because the display RAM is capable of approximately twice the bandwidth of the 68000, the 68000 is usually not delayed by waiting for the display buses to become available.

The 68000 can fetch instructions from:

Display RAM
ROM

The 68000 can read and write data directly to:

Display RAM
Parallel I/O Chips
3 Custom I.C.s
ROM

The 68000 transmits data and control to and from the peripherals via the parallel I/O and the 3 custom chips.

/M is the processor clock to the 68000. C1, C3 and CDAC are used to clock the custom chips and determine the timing of signals to the memory arrays.

## ROM

The ROM contains the kernel and DOS routines; it is 128K × 16.

### Parallel I/O

The 2 multipurpose 8520 I/O chips provide the following:

I/O to and from the parallel port connector
Control lines to and from the joystick/mouse ports
A control line to the front panel LED
Internal control lines
Keyboard control lines, clock and data
Serial port control lines
Floppy disk interface control lines
Internal timers

These 2 chips reside on the 68000 buses and are read and written by the 68000.

### Clocks Generator

The entire computer board is run synchronous to the 3.579545 MHz color clock. This is accomplished by generating a number of submultiple frequencies from the master 28.63636 MHz NTSC (or 28.37516 MHz for PA) crystal oscillator. All clocks are generated by the Fat Agnus custom chip. The following are the primary clocks:

| | |
|---|---|
| C1 | 3.579545 MHz color clock |
| C3 | C2 shifted 45 degrees later |
| 7M | C1 XORed with C3 = 7.15909 MHz |
| CDAC | 7M shifted 90 degrees later |

## The 3 Custom Chips

The 3 custom chips provide very fast manipulation of graphics and audio data in the display RAM. All the major functions in the chips are DMA driven; that is, streams of data are moved between the custom chips and display RAM under DMA control. These streams of data are acted upon by the custom chips. Fat Agnus, custom chip #1, contains 25 dedicated purpose DMA counters.

The 3 chips have control registers which are usually loaded by the 68000. However, Fat Agnus also has the capability of loading control registers in the other 2 custom chips. When Fat Agnus performs a bus cycle, it outputs a code on the Register Address Bus telling the other 2 chips the nature of the bus cycle. This is necessary because many of the bus cycles provide data to or from the other 2 chips, thus they must cooperate appropriately.

In addition to manipulating data in the display RAM, the custom chips output streams of data to the video output circuits and audio output circuits, and they move data to and from the floppy disks and serial port.

Note that the display RAM buses can be completely isolated from the 68000 buses by Fat Agnus and Data Bus drivers. Thus, Fat Agnus can be performing a bus cycle on the display buses simultaneously with the 68000 performing a bus cycle on its buses. This parallelism increases throughout.

## Bus Control, Address/Data MUX, Address Driver

The bus control logic resides in the control chip (GARY) and Fat Agnus. They provide 3 major functions, they:

Synchronize the 68000 to the current phase of C1
Arbitrate between the 68000 and Fat Agnus for the display buses
Generate DRAM timing for the video RAM bus drivers appropriate to the current cycle

Synchronizing the 68000 to C1 is straightforward, since the 68000 is clocked by 7M which is twice the frequency and synchronous to C1. If the 68000 starts a bus cycle in the wrong phase of C1, the bus control chip merely delays /DTACK long enough so that the 68000 will complete the bus cycle in the desired phase relationship to C1. This phase relationship is necessary because the custom chips and the display RAM are clocked by C1.

Arbitration is very simple. Fat Agnus tells the bus control prior to taking the display RAM buses by asserting an input to the control chip (GARY) called / DBR. Whenever Fat Agnus has the display buses and the 68000 wants them, the 68000 is held off by not giving it /DTACK. In this state the 68000 has no effect on the display buses until the bus controller enables the bus drivers.

Fat Agnus generates the DRAM timings and does all address multiplexing. If the 68000 is running a video memory cycle, its addresses are routed through Fat Agnus onto the multiplexed address lines. If the custom chips are running a memory cycle the addresses are routed to the multiplexed address lines from internal address register.

### Display RAM

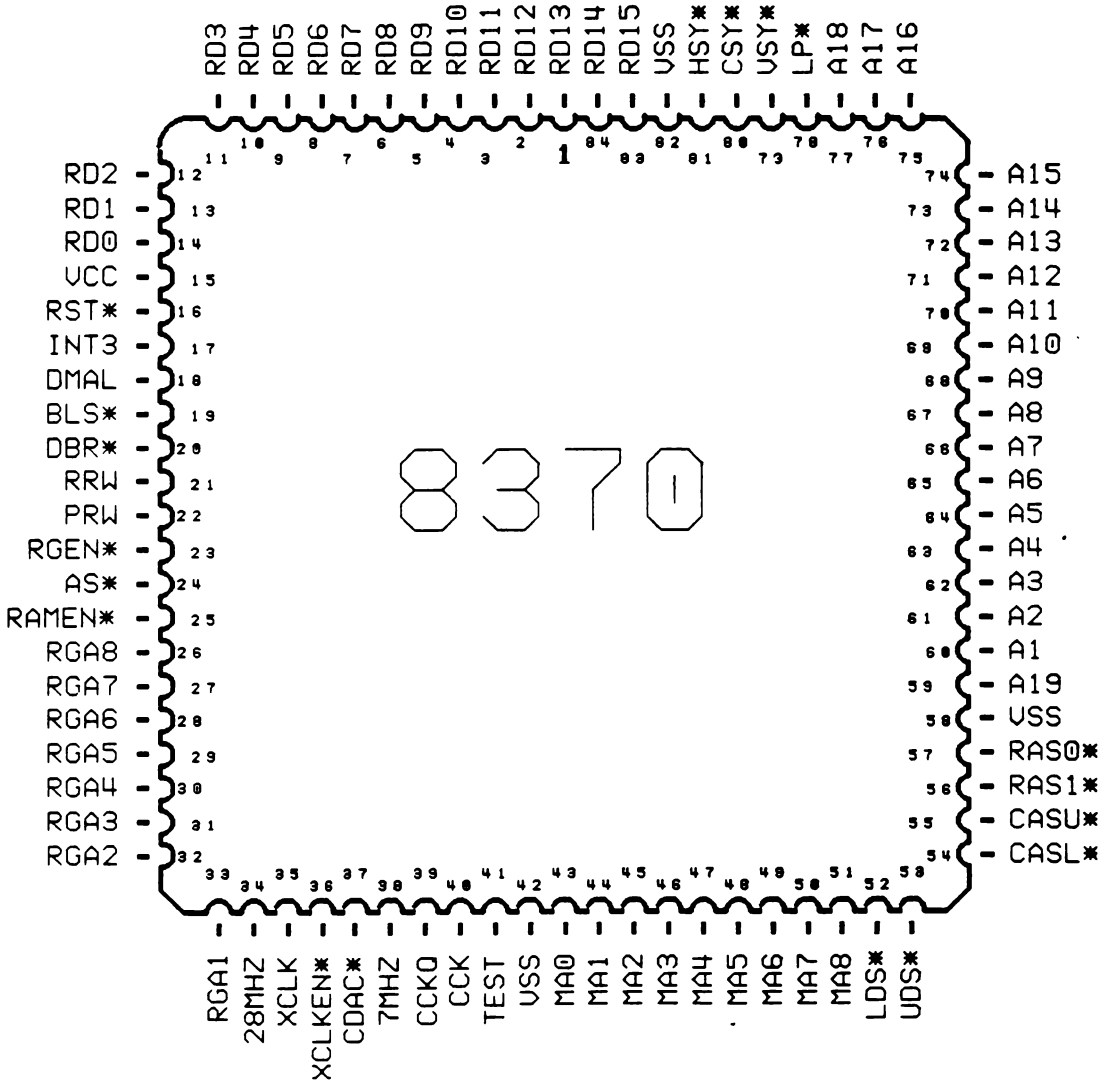
The display RAM is a 512K read/write memory that resides on the RAM address and RAM data buses. It is expandable to 1M bytes by the addition of the RAM expansion module. It is implemented using standard 256K × 1 dynamic RAMs, refreshed by Fat Agnus.

The display RAM is really used for much more than just holding graphics data. It also stores code and data for the 68000.

## Custom Control Chips

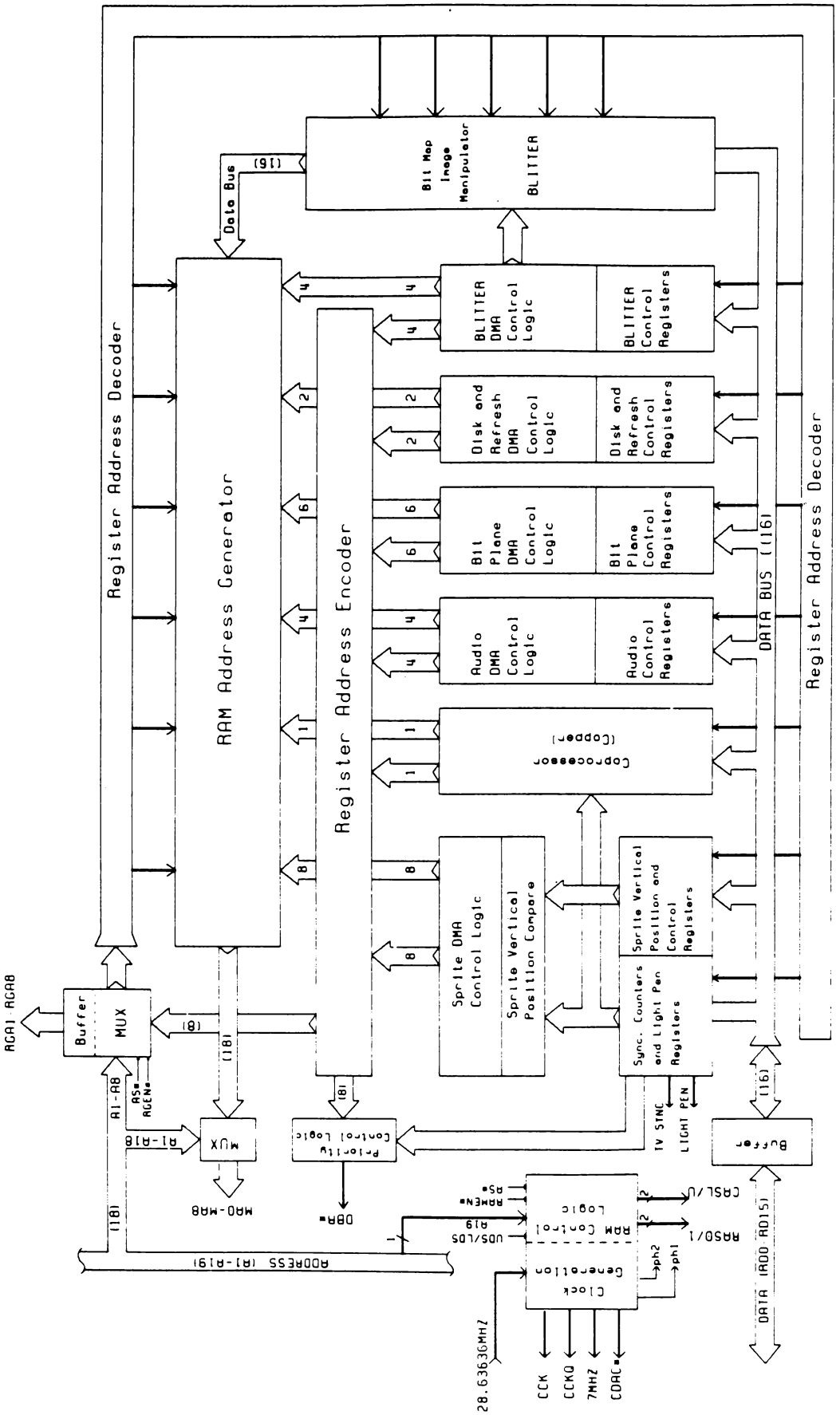
The Amiga's animation, graphics and sound are produced by three custom chips. Fat Agnus (8370), Denise (8362) and Paula (8364). A fourth custom chip, Gary serves as the control chip. The following pages include pin diagrams, feature lists, and block diagrams for these chips.

# Custom Animation Chip
## Fat Agnus




## Features:

- Bit Blitter—Uses hardware to move display data—Allows high speed animation—Frees the CPU for other concurrent tasks
- Display Synchronized Coprocessor
- Controls 25 DMA Channels—Allows the disk and sound to operate with minimal CPU intervention
- Generates all system clocks from the 28 Mhz oscillator
- Generates all control signals for the video RAM and expansion RAM card
- Provides the address to the video and expansion RAM multiplexing

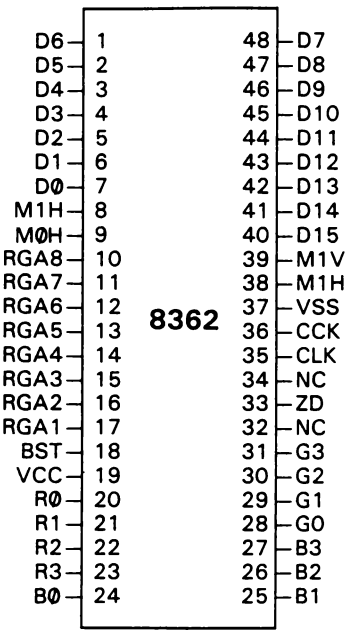



**Fat Agnus Block Diagram**

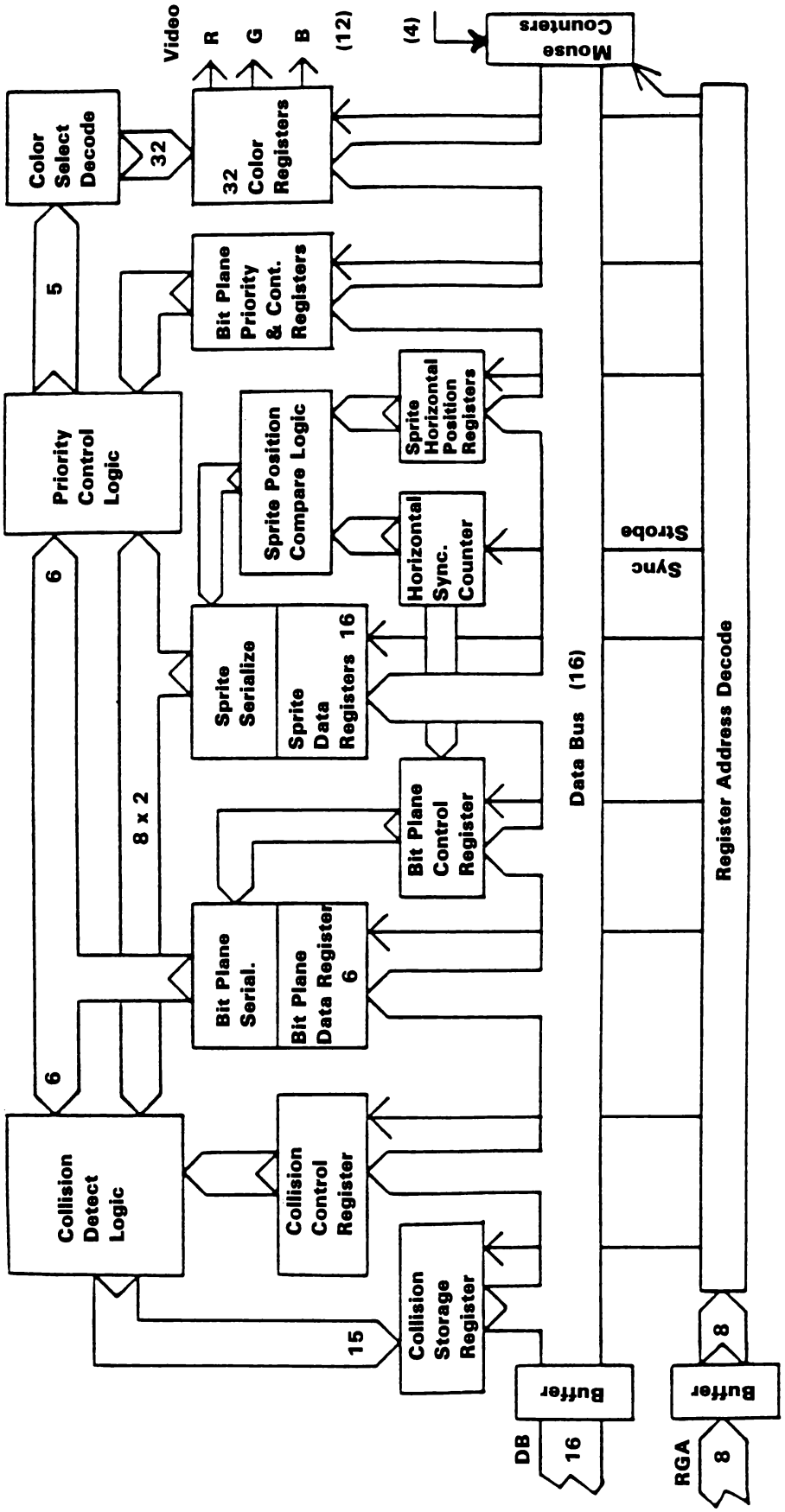
# Custom Graphics Chip
## Denise

## Features:

- Many different resolutions
  320 × 200 up to 640 × 400
- 4096 colors on a TV or RGB monitor
- Eight re-usable sprite controllers
- 60 or 80 column text
- Same software for all TVs and monitors



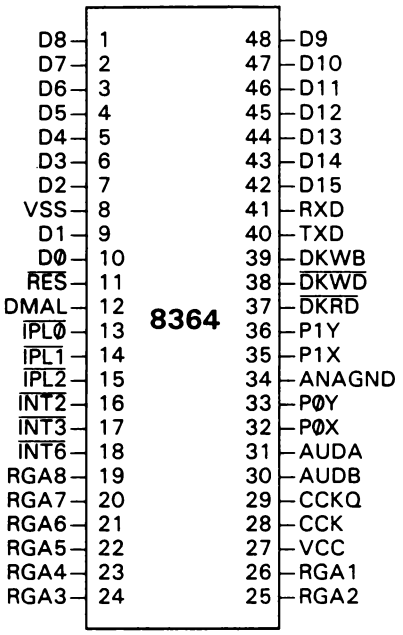

| Pin | Name | Description | Type |
|---|---|---|---|
| 1-7 | D0-D6 | Data Bus Lines 0-6 | I/O |
| 8 | M1H | Mouse 1 Horizontal | I |
| 9 | M0H | Mouse 0 Horizontal | I |
| 10-17 | RGA1-8 | Register Address 1-8 | I |
| 18 | /BURST | Color Burst | O |
| 19 | Vcc | +5 VDC | I |
| 20-23 | R0-3 | Video Red Bit 0-3 | O |
| 24-27 | B0-3 | Video Blue Bit 0-3 | O |
| 28-31 | G0-3 | Video Green Bit 0-3 | O |
| 32 | N/C | No Connection | N/C |
| 33 | /ZD | Background Indicator | O |
| 34 | N/C | No Connection | N/C |
| 35 | 7M | 7.15909 MHz Clock | I |
| 36 | CCK | Color Clock | I |
| 37 | Vss | Ground | I |
| 38 | M0V | Mouse 0 Vertical | I |
| 39 | M1V | Mouse 1 Vertical | I |
| 40-48 | D7-D15 | Data Bus Lines 7-15 | I/O |




Denise Block Diagram

# Custom Sound/Peripherals Chip

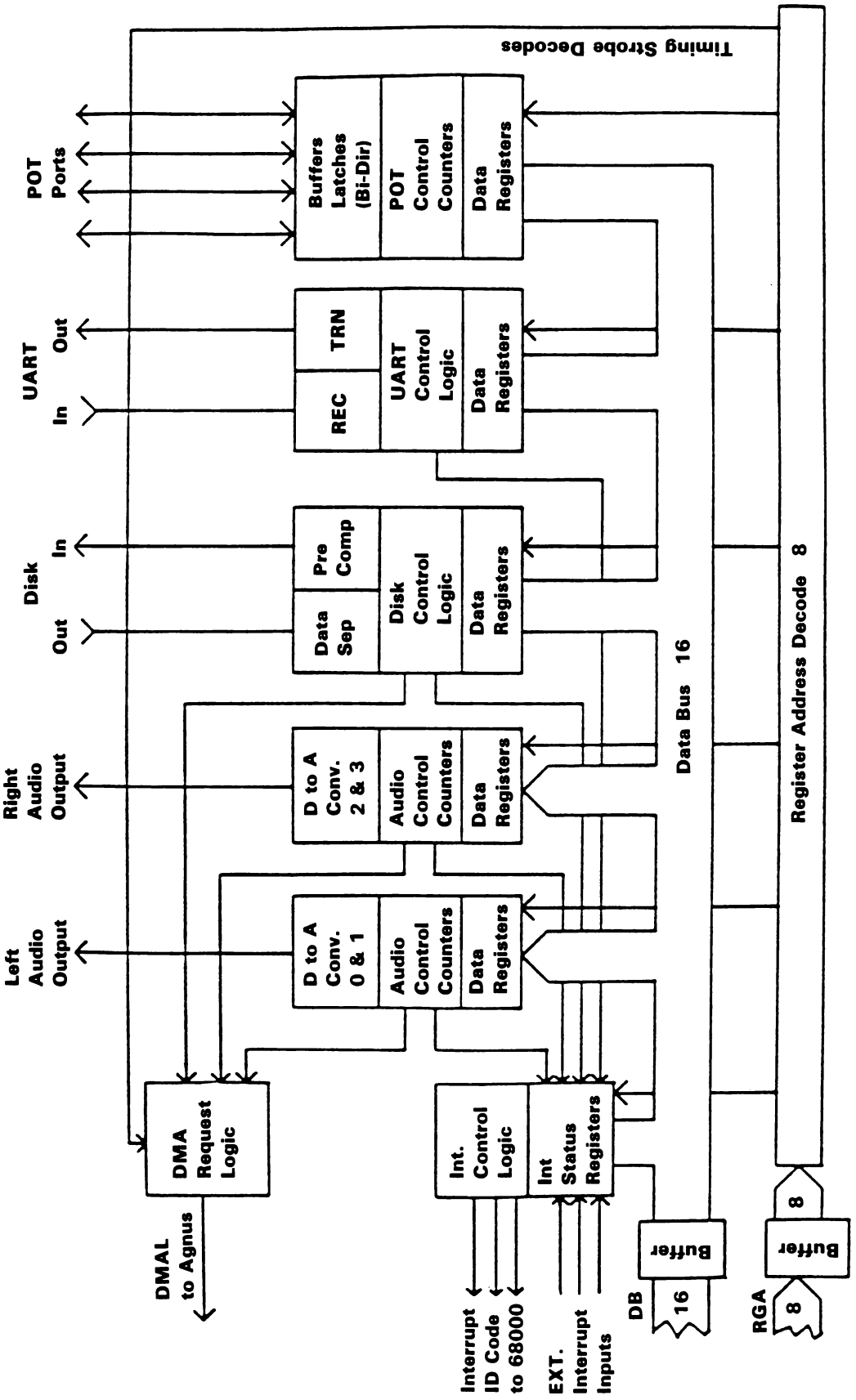
## Paula




## Features:

- Four voices of sound output configured as two stereo channels
- Nine octaves
- Complex waveforms
- Uses both amplitude and frequency modulation
- I/O controls for disk data and controller ports
- Microdisk controller
- Interrupt control system

| Pin | Name | Description | Type |
|---|---|---|---|
| 1-7 | D2-D8 | Data Bus Lines 2-8 | I/O |
| 8 | Vss | Ground | I |
| 9,10 | D0,D1 | Data Bus Lines 0,1 | I/O |
| 11 | /RES | System Reset | I |
| 12 | DMAL | DMA Request Line | O |
| 13-15 | /IPL0-2 | Interrupt Line 0-2 | O |
| 16-18 | /INT2,3,6 | Interrupt Level 2,3,6 | I |
| 19-26 | RGA1-8 | Register Address 1-8 | I |
| 27 | Vcc | +5 VDC | I |
| 28 | CCK | Color Clock | I |
| 29 | CCKQ | Color Clock Delay | I |
| 30 | AUDB | Right Audio | O |
| 31 | AUDA | Left Audio | O |
| 32 | POT0X | Pot 0X | I/O |
| 33 | POT0Y | Pot 0Y | I/O |
| 34 | VSSANA | Analog Ground | I |
| 35 | POT1X | Pot 1X | I/O |
| 36 | POT1Y | Pot 1Y | I/O |
| 37 | /DKRD | Disk Read Data | I |
| 38 | /DKWD | Disk Write Data | O |
| 39 | DKWE | Disk Write Enable | O |
| 40 | TXD | Serial Transmit Data | O |
| 41 | RXD | Serial Receive Data | I |
| 42-48 | D9-15 | Data Bus Lines 9-15 | I/O |

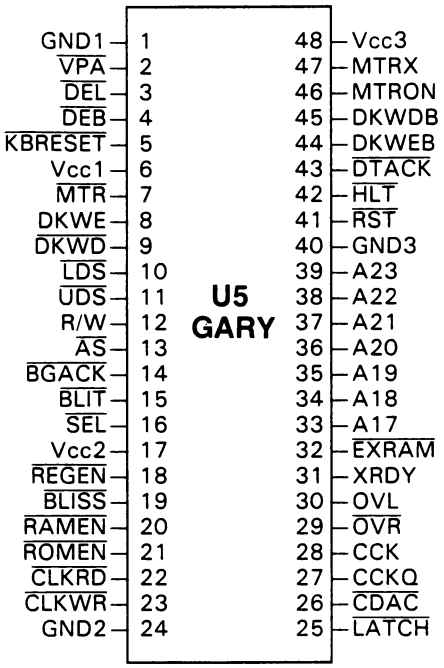



Paula Block Diagram

# Custom Control Chip
## Gary

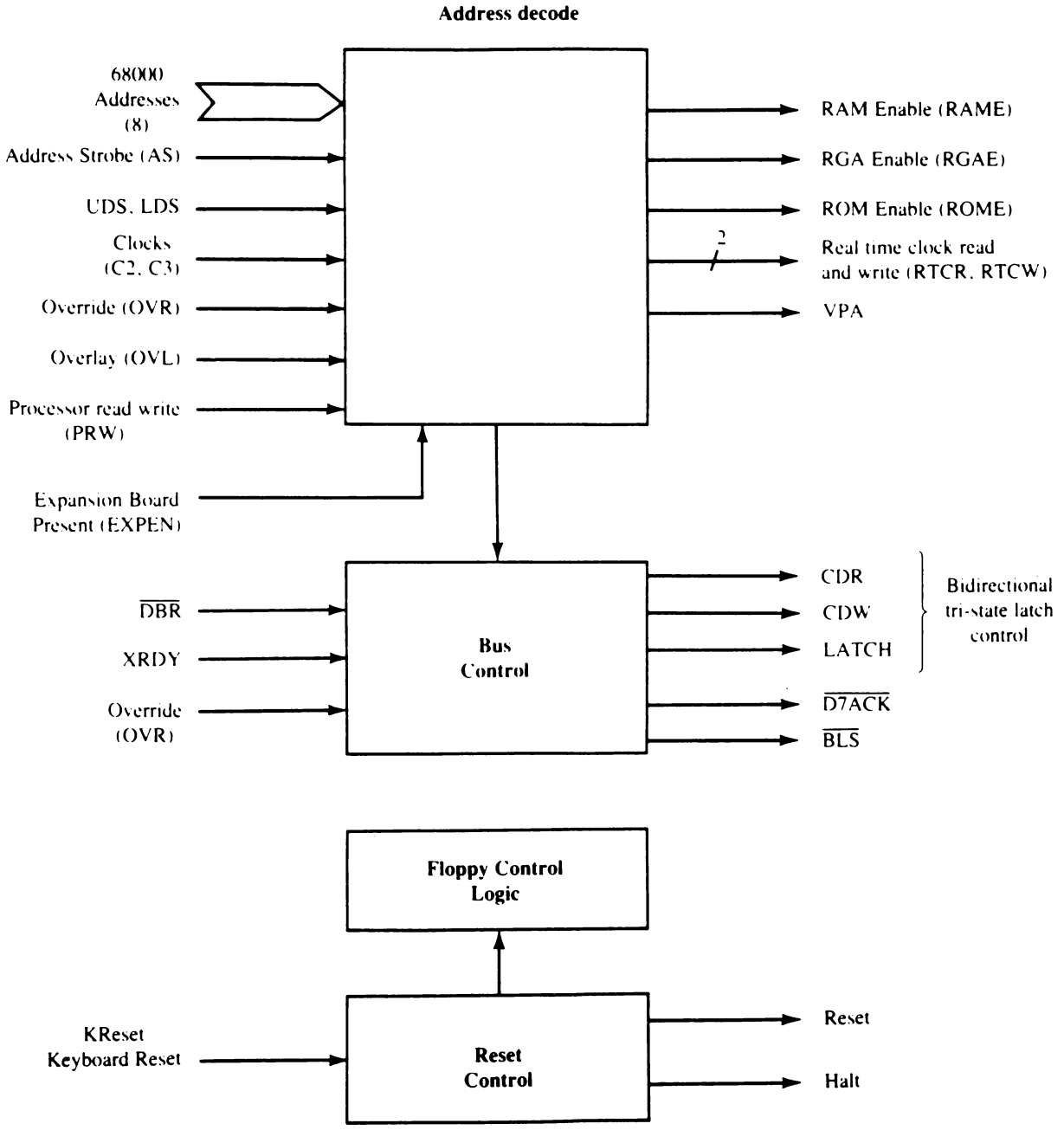
## Features:

- Provides all bus control signals.
- Provides all address decoding.
- Generates the 68000 VPA signal.
- Handles some of the floppy circuitry.
- Provides keyboard reset interface.

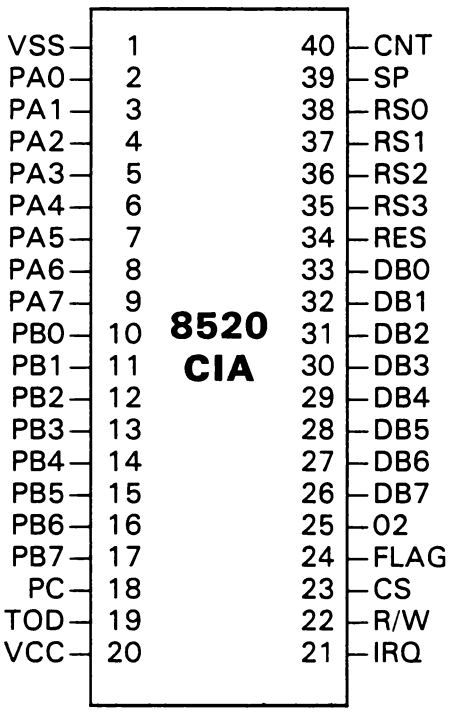



**For signal descriptions see Schematic #312511 (sheet 1 of 9)**

# Gary Block Diagram



# Complex Interface Adapter




## INTERFACE SIGNALS

### 02 Clock Input

The 02 clock is a TTL, compatible input used for internal device operation and as a timing reference for communicating with the system data bus.

### CS — Chip Select Input

The CS input controls the activity of the 8520. A low level on CS while 02 is high causes the device to respond to signals on the R/W and address (RS) lines. A high on CS prevents these lines from controlling the 8520. The CS line is normally activated (low) at 02 by the appropriate address combination.

### R/W — Read/Write Input

The R/W signal is normally supplied by the microprocessor and controls the direction of data transfers of the 8520. A high on R/W indicates a read (data transfer out of the 8520), while a low indicates a write (data transfer into the 8520).

### RS3-RS0 — Address Inputs

The address inputs select the internal registers as described by the Register Map.

### DB7-DB0 — Data Bus Inputs/ Outputs

The eight bit data bus transfers information between the 8520 and the system data bus. These pins are high impedance inputs unless CS is low and R/W and 02 are high, to read the device. During this read, the data bus output buffers are enabled, driving the data from the selected register onto the system data bus.

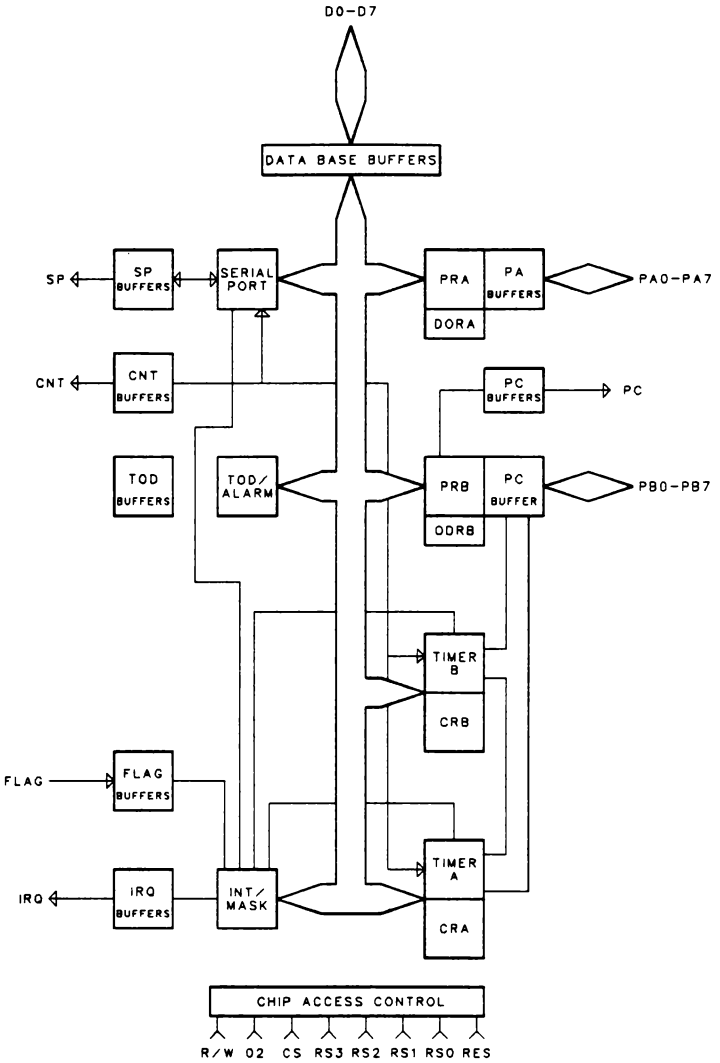
### IRQ — Interrupt Request Output

IRQ is an open drain output normally connected to the processor interrupt input. An external pullup resistor holds the signal high, allowing multiple IRQ-outputs to be connected together. The IRQ output is normally off (high impedance) and is activated low as indicated in the functional description.

### RES — Reset Input

A low on the RES pin resets all internal registers. The port pins are set as inputs and port registers to zero (although a read of the ports will return all highs because of passive pullups). The timer control registers are set to zero and the timer latches to all ones. All other registers are reset to zero.

## REGISTER MAP




| RS3 | RS2 | RS1 | RS0 | REG | | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | PRA | Peripheral Data Reg. A |
| 0 | 0 | 0 | 1 | 1 | PRB | Peripheral Data Reg. B |
| 0 | 0 | 1 | 0 | 2 | DDRA | Data Direction Reg. A |
| 0 | 0 | 1 | 1 | 3 | DDRB | Data Direction Reg. B |
| 0 | 1 | 0 | 0 | 4 | TA LO | Timer A Low Register |
| 0 | 1 | 0 | 1 | 5 | TA HI | Timer A High Register |
| 0 | 1 | 1 | 0 | 6 | TB LO | Timer B Low Register |
| 0 | 1 | 1 | 1 | 7 | TB HI | Timer B High Register |
| 1 | 0 | 0 | 0 | 8 | | Event LSB |
| 1 | 0 | 0 | 1 | 9 | | Event 8-15 |
| 1 | 0 | 1 | 0 | A | | Event MSB |
| 1 | 0 | 1 | 1 | B | | No Connect |
| 1 | 1 | 0 | 0 | C | SDR | Serial Data Register |
| 1 | 1 | 0 | 1 | D | ICR | Interrupt Control Register |
| 1 | 1 | 1 | 0 | E | CRA | Control Register A |
| 1 | 1 | 1 | 1 | F | CRB | Control Register B |

## FUNCTION DESCRIPTION

### I/O Ports (PRA, PRB, DDRA, DDRB)

Ports A and B each consist of an 8-bit Peripheral Data Register (PR) and an 8-bit Data Direction Register (DDR). If a bit in the DDR is set to the corresponding bit in the PR it is an output. If a DDR bit is set to zero, the corresponding PR bit is defined an an input. On a READ, the PR reflects the information present on the actual port pins (PA0-PA7, PBO-PB7) for both input and output bits. Port A has both passive and active pullup devices, providing both CMOS and TTL compatibility. It can drive 2 TTL loads. Port B has only passive pullup device and has a much higher current-sinking capability.

### Handshaking

Handshaking on data transfers can be accomplished using the PC output pin and the FLAG input pin. PC will go low on the 3rd cycle after a PORT B access. This signal can be used to indicate "data ready" at PORT B or "data accepted" from PORT B. Handshaking on a 16-bit data transfers (using both PORT A and PORT B) is possible by always reading or writing PORT A first. FLAG is a negative edge sensitive input which can be used for receiving the PC output from another 8520 or as a general purpose interrupt input. Any negative transition on FLAG will set the FLAG interrupt bit.

| Reg | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | PRA | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| 1 | PPB | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| 2 | DDRA | DPA7 | DPA6 | DPA5 | DPA4 | DPA3 | DPA2 | DPA1 | DPA0 |
| 3 | DDRB | DPB7 | DPB6 | DPB5 | DPB4 | DPB3 | DPB2 | DPB1 | DPB0 |

### Interval Timers (Timer A, Timer B)

Each interval timer consists of a 16-bit read-only Timer Counter and a 16-bit write-only Timer Latch. Data written to the timer is latched in the Timer Latch, while data read from the timer are the present contents of the Timer Counter. The timers can be used independently or linked for extended operations. The various timer modes allow generation of long time delays, variable width pulses, pulse trains and variable frequency waveforms. Utilizing the CNT input, the timers can count external pulses or measure frequency, pulse width and delay times of external signals. Each timer has an associated control register, providing independent control of the following functions.

### Start/Stop

A control bit allows the timer to be started or stopped by the microprocessor at any time.

### PB On/Off

A control bit allows the timer output to appear on a PORT B output line (PB6 for TIMER A and PB7 for TIMER B). This function overrides the DDRB control bit and forces the appropriate PB line to an output.

### Toggle/Pulse

A control bit selects the output applied to PORT B. On every timer underflow the output can either toggle or generate a single positive pulse of one cycle duration. The toggle output is set high whenever the timer is started and is set low by RES.

### One-Shot/Continuous

A control bit selects either timer mode. In one-shot mode, the timer will count down form the latched value to zero, generate an interrupt, reload the latched value, then stop. In continuous mode, the timer will count from the latched value to zero, generate an interrupt, reload the latched value and repeat the procedure continuously. In one-shot mode: a write to Timer High (registers 5 for TIMER A, 7 for TIMER B) will transfer the timer latch to the counter and inititate counting regardless of the start bit.

### Force Load

A strobe bit allows the timer latch to be loaded into the timer counter at any time, whether the timer is running or not.

### Input Mode

Control bits allow selection of the clock used to decrement the timer. TIMER A can count 02 pulses or external pulses applied to the CNT pin. TIMER B can count 02 pulses, external CNT pulses, TIMER A underflow pulses or TIMER A underflow pulses while the CNT pin is held high.

The timer latch is loaded into the timer on any timer underflow, on a force load or following a write to the high byte of the prescaler while the timer is stopped. If the timer is running, a write to the high byte will load the timer latch, but not reload the counter.

**READ (TIMER)**

| REG | Name | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 4 | TA LO | TAL7 | TAL6 | TAL5 | TAL4 | TAL3 | TAL2 | TAL1 | TAL0 |
| 5 | TA HI | TAH7 | TAH6 | TAH5 | TAH4 | TAH3 | TAH2 | TAH1 | TAH0 |
| 6 | TB LO | TBL7 | TBL6 | TBL5 | TBL4 | TBL3 | TBL2 | TBL1 | TBL0 |
| 7 | TB HI | TBH7 | TBH6 | TBH5 | TBH4 | TBH3 | TBH2 | TBH1 | TBH0 |

**WRITE (PRESCALER)**

| REG | Name | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 4 | TA LO | PAL7 | PAL6 | PAL5 | PAL4 | PAL3 | PAL2 | PAL1 | PAL0 |
| 5 | TA HI | PAH7 | PAH6 | PAH5 | PAH4 | PAH3 | PAH2 | PAH1 | PAH0 |
| 6 | TB LO | PBL7 | PBL6 | PBL5 | PBL4 | PBL3 | PBL2 | PBL1 | PBL0 |
| 7 | TB HI | PBH7 | PBH6 | PBH5 | PBH4 | PBH3 | PBH2 | PBH1 | PBH0 |

## TOD

TOD consists of a 24 bit binary counter. Positive edge transitions on this pin cause the binary counter to increment. The TOD pin has a passive pull-up on it. A programmable ALARM is provide for generating an interrupt at a desired time. The ALARM registers are located at the same addresses as the corresponding TOD register. Access to the ALARM is governed by a Control Register bit. The ALARM is write-only; any read of a TOD address will read time regardless of the state of the ALARM access bit.

A specific sequence of events must be followed for proper setting and reading of TOD. TOD is automatically stopped whenever a write to the register occurs. The clock will not start again until after a write to the LSB Event Register. This assures TOD will always start at the desired time. Since a carry from one stage to the next can occur at any time with respect to a read operation, a latching function is include to keep all Time of Day information constant during a read sequence. All TOD registers latch on a read of MSB event and remain latched until after a read of LSB Event. The TOD clock continues to count when the output registers are latched. If only one register is to be read, there is no carry problem and the register can be read "on the fly", provided that any read of MSB Event is followed by a read of LSB Event to disable the latching.

**READ**

| REG | Name | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 8 | LSB Event | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| 9 | Event 8-15 | E15 | E14 | E13 | E12 | E11 | E10 | E9 | E8 |
| A | MSB Event | E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |

WRITE
CRB7 = 0
CRB7 = 1 ALARM
(SAME FORMAT AS READ)

### Serial Port (SDR)

The serial port is a buffered, 8-bit synchronous shift register system. A control bit selects input or output mode. In input mode, data on the SP pin is shifted into the shift register on the rising edge of the signal applied to the CNT pin. After 8 CNT pulses, the data in the shift register is dumped into the Serial Data Register and an interrupt is generated. In the output mode, TIMER A is used for the baud rate generator. Data is shifted out on the SP pin at 1/2 the underflow rate of TIMER A. The maximum baud rate possible is 02 divided by 6, but the maximum useable baud rate will be determined by line loading and the speed at which the receiver responds to input data. Transmission will start following a write to the Serial Data Register (provided TIMER A is running and in continuous mode). The clock signal derived from TIMER A appears as an output on the CNT pin. The data in the Serial Data Register will be loaded into the shfit register then shift out to the SP pin when a CNT pulse occurs. Data shifted out becomes valid on the falling edge of CNT and remains valid until the next falling edge. After 8 CNT pulses, an interrupt is generated to indicate more data can be sent. If the Serial Data Register was loaded with new information prior to this interrupt, the new data will automatically be loaded into the shift register and transmission will be continuous. If no further data is to be transmitted, after the 8th CNT pulse, CNT will return high and SP will remain at the level of the last data bit transmitted. SDR data is shifted out MSB first and serial input data should also appear in this format.

The bidirectional capability of the Serial Port and CNT clock allows several devices to be connected to a common serial communication bus on which one acts as a master, sourcing data and shift clock, while all other chips act as slaves. Both CNT and SP outputs are open drain, with passive pull-ups, to allow such a common bus. Protocol for slave/master selection can be transmitted over the serial bus, or via dedicated handshaking lines.

| REG | Name | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| C | SDR | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

### Interrupt Control (ICR)

There are five sources of interrupts on the 8520: underflow from TIMER A, underflow from TIMER B, TOD ALARM, Serial Port full/empty and FLAG. A single register provides masking and interrupt information. The Interrupt Control Register consists of a write-only MASK register and a read-only DATA register. Any interrupt which is enabled by the MASK register will set the IR bit (MSB) of the DATA register and bring the IRQ pin low. In a multi-chip system, the IR bit can be polled to detect which chip has generated an interrupt request.

The interrupt DATA register is cleared and the IRQ line returns high following a read of the DATA register. Since each interrupt sets an interrupt bit regardless of the MASK, and each interrupt bit can be selectively masked to prevent the generation of a processor interrupt, it is possible to intermix polled interrupts with true interrupts. However, polling the IR bit will cause the DATA register to clear, therefore, it is up to the user to preserve the information contained in the DATA register if any polled interrupts were present.

The MASK register provides convenient control of individual mask bits. When writing to the MASK register, if bit 7 (SET/CLEAR) of the data written is a ZERO, any mask bit written with a one will be cleared, while those mask bits written with a zero will be unaffected. If bit 7 of the data written is a ONE, any mask bit written with a one will be set, while those mask bits written with a zero will be unaffected. In order for an interrupt flag to set IR and generate an Interrupt Request, corresponding MASK bit must be set.

**READ (INT DATA)**

| REG | Name | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| D | IRC | IR | 0 | 0 | FLG | SP | ALRM | TB | TA |

**WRITE (INT MASK)**

| REG | Name | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| D | IRC | S/C | X | X | FLG | SP | ALRM | TB | TA |

### Control Registers

There are two control registers in the 8520: CRA and CRB. CRA is associated with TIMER A and CRB is associated with TIMER B.

**CRA:**

| BIT | NAME | FUNCTION |
|---|---|---|
| 0 | START | 1 = START TIMER A, 0 = STOP TIMER A. This bit is automatically reset when underflow occurs during one-shot mode. |
| 1 | PBON | 1 = TIMER A output appears on PB6, 0 = PB6 normal operation. |
| 2 | OUTMODE | 1 = TOGGLE, 0 = PULSE |
| 3 | RUNMODE | 1 = ONE-SHOT, 0 = CONTINUOUS |
| 4 | LOAD | 1 = FORCE LOAD (this is a STROBE input, there is no data storage, bit 4 will always read back a zero and writing a zero has no effect. |
| 5 | INMODE | 1 = TIMER A counts positive CNT transitions, 0 = TIMER A counts 02 pulses. |
| 6 | SPMODE | 1 = SERIAL PORT output (CNT sources shift clock). 0 = SERIAL PORT input (external shift clock required). |
| 7 | TODIN | 1 = 50 Hz clock required on TOD pin for accurate time.<br>0 = 60 Hz clock required on TOD pin for accurate time. |

**CRB:**

| BIT | NAME | FUNCTION |
|---|---|---|
| | | (Bits CRB0-CRB4 are identical to CRA0-CRA4 for TIMER B with the exception that bit 1 controls the output of TIMER B on PB7). |
| 5.6 | INMODE | Bits CRB5 and CRB6 select one of four input modes for TIMER B as: |

| CRB6 | CRB5 | |
|---|---|---|
| 0 | 0 | TIMER B counts 02 pulses. |
| 0 | 1 | TIMER B counts positive CNT transitions. |
| 1 | 0 | TIMER B counts TIMER A underflow pulses. |
| 1 | 1 | TIMER B counts TIMER A underflow pulses while CNT is high. |

| | | |
|---|---|---|
| 7 | ALARM | 1 = writing to TOD registers set ALARM, 0 = writing to TOD registers sets TOD clock. |

## ELECTRICAL PARAMETERS

### Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the circuit. Functional operation of the device at these or any conditions other than those indicated in the operating conditions of the specification is not implied. Exposure to the maximum ratings for extended periods may adversely affect device reliability.

| | | | | | |
|---|---|---|---|---|---|
| Supply Voltage | Vcc | −0.3V to 7.0V | Operating Temp. | Top | 0°C to 70°C |
| Input/Output Voltage | Vin | −0.3V to 7.0V | Storage Temp. | Tstg | −55°C to 150°C |

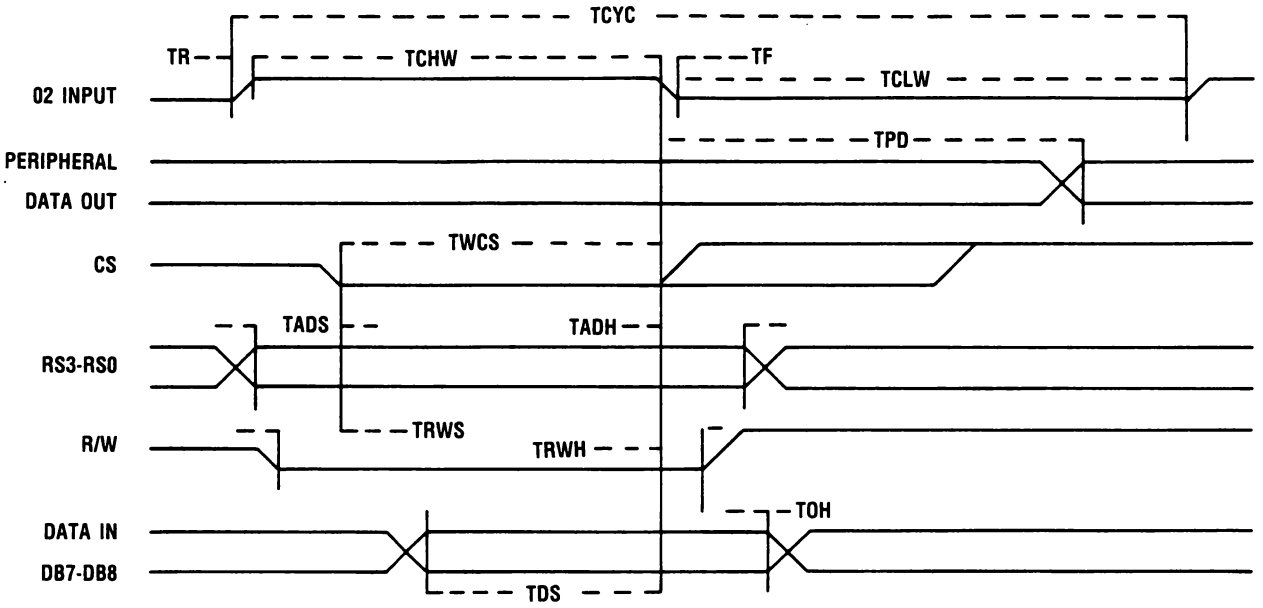
*All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

**ELECTRICAL CHARACTERISTICS (VCC +/− 5%, VSS = 0v, TA = 0.70 C)**

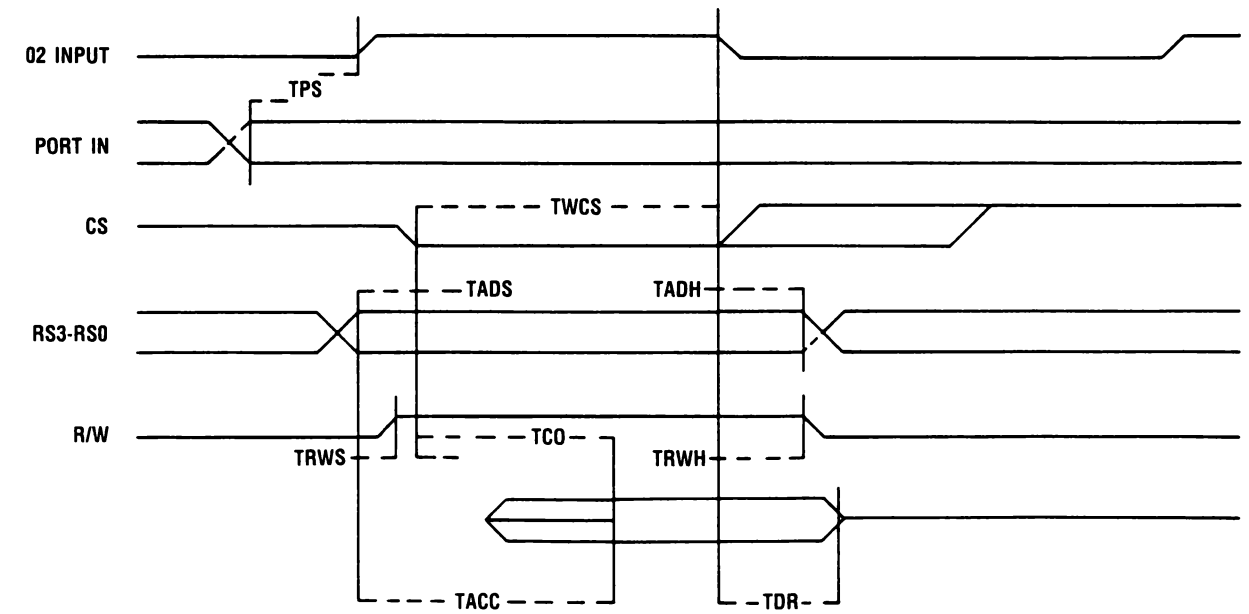
| CHARACTERISTICS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Input High Voltage | Vih | +2.4 | — | Vcc | V |
| Input Low Voltage | Vil | −3.0 | — | +0.8 | V |
| Input leakage current VIN = VSS + 5V (TOD, R/W, 02, RES, RS0-RS3, CS) | Iin | — | 1.0 | 2.5 | μA |
| PA0-7, PB0-7, TOD, FLAG, SP, CNT | Rpi | 3.1 | 5.0 | — | KΩ |
| Output leakage current for High Impedance State VIN = 4V to 2.4V (DB0-DB7, IRQ) | Itsi | — | ±1.0 | ±10.0 | μA |
| Output High Voltage VCC = MIN, LOAD < −200μA (PA0-PA7, DB0-DB7) | Voh | +2.4 | — | Vcc | V |
| Output Low Voltage (PA0-PA7, DB0-DB7) VCC = MIN, LOAD<3.2μA | Vol | — | — | +0.40 | V |
| Output High Current (sourcing) VOH>2.4V (PA0-PA7, DB0-DB7) | Ioh | −200 | −1000 | — | μA |
| Output Low Current (sinking) VOL<.4V (PA0-PA7, DB0-DB7) | Iol | 3.2 | — | — | μA |
| Output Low Current (sinking) VOL<.4V (PC, PB0-PB7) | Iol | 13.0 | — | — | μA |
| Input Capacitance | Cin | — | 7 | 10 | pf |
| Output Capacitance | Cout | — | 7 | 10 | pf |
| Power Supply Current | Icc | — | 70 | 100 | μA |

## TIMING DIAGRAMS

WRITE TIMING DIAGRAM




READ TIMING DIAGRAM



## 2.2 Timing Characteristics

| SYMBOL | CHARACTERISTIC | 1MHZ MIN | 1MHZ MAX |
|---|---|---|---|
| | **02 CLOCK** | | |
| TCYC | Cycle Time | 1000 | 10,000 |
| TR, TF | Rise and Fall Time | — | 25 |
| TCHW | Clock Pulse Width (High) | 440 | 5,000 |
| TCLW | Clock Pulse Width (Low) | 440 | 5,000 |
| | **WRITE CYCLE** | | |
| TPD | Output Delay From 02 | — | 960 |
| TWCS | CS low while 02 high | 280 | — |
| TADS | Address setup time | 58 | — |
| TADH | Address hold time | 10 | — |
| TRWS | R/W setup time | 58 | — |
| TRWH | R/W hold time | 10 | — |
| TDS | Data bus setup time | 200 | — |
| TDH | Data bus hold time | 15 | — |
| | **READ CYCLE** | | |
| TPS | Port setup time | 300 | — |
| TWCS(2) | CS low while 02 high | 280 | — |
| TADS | Address setup time | 58 | — |
| TADH | Address hold time | 10 | — |
| TRWS | R/W setup time | 58 | — |
| TRWH | R/W hold time | 10 | — |
| TACC | Data access from RS3-RS0 | — | 300 |
| TCO(3) | Data access from CS | — | 240 |
| TDR | Data release time | 50 | — |

*See diagram on page 23 for timing relationships.

*NOTES:

1. All timings are referenced from VIL max and VIH min on inputs and VOL max and VOH min on outputs.
2. TWCS is measured from the later of 02 high or CS low. CS must be low at least until the end of 02 high.
3. TCO is measured from the later of 02 high or CS low. Valid data is available only after the later of TACC of TCO.

# Input/Output Connectors

This section lists pin assignments for several input/output connectors on the Amiga. The information in this section is highly technical and is intended only for those expert in connecting external devices to computers. You do not need this information if you use a cable specifically designed for use with the Amiga and the add-on you want to connect.

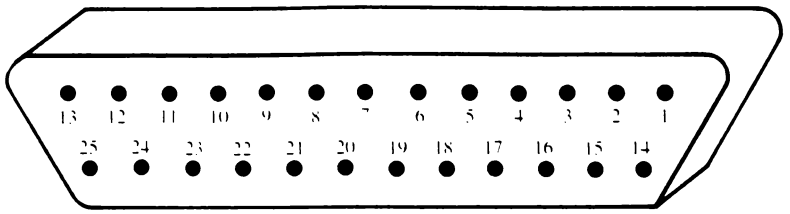
For information about connectors not described in this section, see the *Amiga Hardware Manual*.

*If you attach peripherals with cables other than those designed for use with the Amiga, note:* **some pins on Amiga connectors provide power outputs and non-standard signals. Attempting to use cables not wired specifically for the Amiga may cause damage to the Amiga or to the equipment you connect.** The descriptions below include specific warnings for each connector. For more information about connecting add-ons, consult your Amiga dealer.

In the descriptions that follow, an asterisk (*) at the end of a signal name indicates a signal that is active low.

## Serial Connector

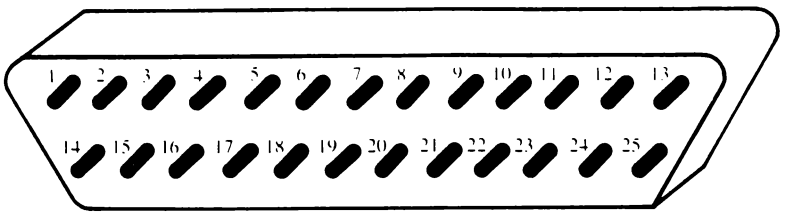
In the following table, the second column from the left gives the Amiga pin assignments. The third and fourth columns from the left give pin assignments for other commonly used connections; the information in these two columns is given for comparison only.




**WARNING: Pins 9 and 10 on the Amiga serial connector are used for external power. Connect these pins ONLY if power from them is required by the external device.** The table lists the power provided by each of these pins.

| Pin | Amiga 500 | RS232 | HAYES® | Description |
|---|---|---|---|---|
| 1 | GND | GND | GND | FRAME GROUND |
| 2 | TXD | TXD | TXD | TRANSMIT DATA |
| 3 | RXD | RXD | RXD | RECEIVE DATA |
| 4 | RTS | RTS | | REQUEST TO SEND |
| 5 | CTS | CTS | CTS | CLEAR TO SEND |
| 6 | DSR | DSR | DSR | DATA SET READY |
| 7 | GND | GND | GND | SYSTEM GROUND |
| 8 | DCD | DCD | DCD | CARRIER DETECT |
| 9 | +12V | | | +12 VOLT CARRIER |
| 10 | −12V | | | −12 VOLT CARRIER |
| 11 | AUDO | | | AUDIO OUT OF AMIGA |
| 12 | | S.SD | SI | SPEED INDICATE |
| 13 | | S.CTS | | |
| 14 | | S.TXD | | |
| 15 | | TXC | | |
| 16 | | S.RXD | | |
| 17 | | RXC | | |
| 18 | AUDI | | | AUDIO INTO AMIGA |
| 19 | | S.RTS | | |
| 20 | DTR | DTR | DTR | DATA TERMINAL READY |
| 21 | | SQD | | |
| 22 | RI | RI | RI | RING INDICATOR |
| 23 | | SS | | |
| 24 | | TXC1 | | |
| 25 | | | | |

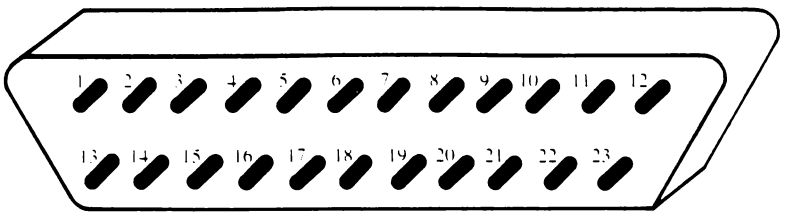
## A500 Parallel Connector




**WARNING: Pin 14 on the Amiga parallel connector supplies +5 volts of power. Connect this pin ONLY if the power from it is required by the external device. NEVER connect this pin to an output of an external device or to a signal ground. Pins 17-25 are for grounding signals. DO NOT connect these pins directly to a shield ground.**

| Pin | Name | Description |
|---|---|---|
| 1 | STROBE* | STROBE |
| 2 | D0 | DATA BIT 0 (Least sign. bit) |
| 3 | D1 | DATA BIT 1 |
| 4 | D2 | DATA BIT 2 |
| 5 | D3 | DATA BIT 3 |
| 6 | D4 | DATA BIT 4 |
| 7 | D5 | DATA BIT 5 |
| 8 | D6 | DATA BIT 6 |
| 9 | D7 | DATA BIT 7 |
| 10 | ACK* | ACKNOWLEDGE |
| 11 | BUSY | BUSY |
| 12 | POUT | PAPER OUT |
| 13 | SEL | SELECT |
| 14 | +5V PULLUP | +5 VOLTS POWER (100 mA) |
| 15 | NC | NO CONNECTION |
| 16 | RESET* | RESET |
| 17 | GND | SIGNAL GROUND |
| 18 | GND | SIGNAL GROUND |
| 19 | GND | SIGNAL GROUND |
| 20 | GND | SIGNAL GROUND |
| 21 | GND | SIGNAL GROUND |
| 22 | GND | SIGNAL GROUND |
| 23 | GND | SIGNAL GROUND |
| 24 | GND | SIGNAL GROUND |
| 25 | GND | SIGNAL GROUND |

## RGB Monitor Connector

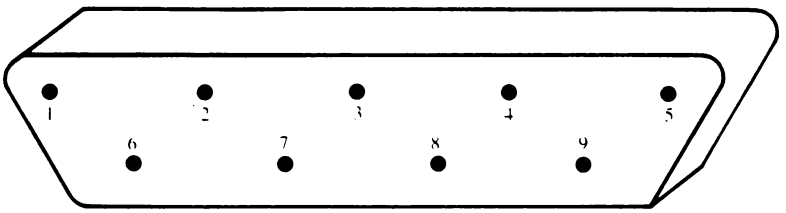



**WARNING: Pins 21, 22, and 23 on the RGB monitor connector are used for external power. Connect these pins ONLY if power from them is required by the external device.** The table lists the power provided by each of these pins.

| Pin | Name | Description |
|---|---|---|
| 1 | XCLK* | EXTERNAL CLOCK |
| 2 | XCLKEN* | EXTERNAL CLOCK ENABLE |
| 3 | RED | ANALOG RED |
| 4 | GREEN | ANALOG GREEN |
| 5 | BLUE | ANALOG BLUE |
| 6 | DI | DIGITAL INTENSITY |
| 7 | DB | DIGITAL BLUE |
| 8 | DG | DIGITAL GREEN |
| 9 | DR | DIGITAL RED |
| 10 | CSYNC* | COMPOSITE SYNC |
| 11 | HSYNC* | HORIZONTAL SYNC |
| 12 | VSYNC* | VERTICAL SYNC |
| 13 | GNDRTN | RETURN FOR XCLKEN* |
| 14 | ZD* | ZERO DETECT |
| 15 | C1* | CLOCK OUT |
| 16 | GND | GROUND |
| 17 | GND | GROUND |
| 18 | GND | GROUND |
| 19 | GND | GROUND |
| 20 | GND | GROUND |
| 21 | −12V | −12 VOLTS POWER (50 mA) |
| 22 | +12V | +12 VOLTS POWER (100 mA) |
| 23 | +5V | +5 VOLTS POWER (100 mA) |

# Mouse/Game Controller Connectors

There are connectors labeled "JOY1" and "JOY2" on the back of the Amiga 500. If you use a mouse to control the Workbench, you must attach it to connector JOY 1. You can attach joystick controllers to either of the connectors. To use a light pen, you must attach it to connector 1. The following tables describe mouse, game controller, and light pen connections.




**WARNING: Pin 7 on each of these connectors supplies +5 volts of power. Connect this pin ONLY if power from it is required by the external device.**

## Connectors 1 and 2: Mouse Connections

| Pin | Name | Description |
|---|---|---|
| 1 | MOUSE V | MOUSE VERTICAL |
| 2 | MOUSE H | MOUSE HORIZONTAL |
| 3 | MOUSE VQ | VERTICAL QUADRATURE |
| 4 | MOUSE HQ | HORIZONTAL QUADRATURE |
| 5 | MOUSE BUTTON 2 | MOUSE BUTTON 2 |
| 6 | MOUSE BUTTON 1 | MOUSE BUTTON 1 |
| 7 | +5V | +5 VOLTS POWER (100 mA) |
| 8 | GND | GROUND |
| 9 | MOUSE BUTTON 3 | MOUSE BUTTON 3 |

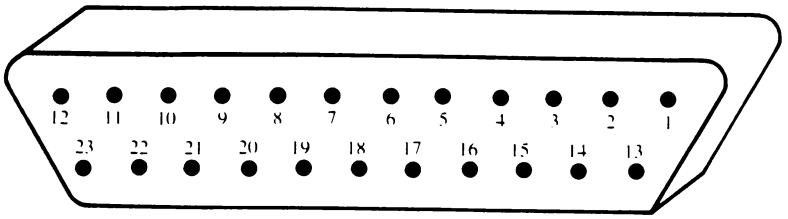
## Connectors 1 and 2: Game Controller

| Pin | Name | Description |
|---|---|---|
| 1 | FORWARD* | CONTROLLER FORWARD |
| 2 | BACK* | CONTROLLER BACK |
| 3 | LEFT* | CONTROLLER LEFT |
| 4 | RIGHT* | CONTROLLER RIGHT |
| 5 | POT X | HORIZONTAL POTENTIOMETER |
| 6 | FIRE* | CONTROLLER FIRE |
| 7 | +5V | +5 VOLTS POWER (100 mA) |
| 8 | GND | GROUND |
| 9 | POT Y | VERTICAL POTENTIOMETER |

## Connector 2: Light Pen Connection

| Pin | Name | Description |
|---|---|---|
| 1 | | |
| 2 | | |
| 3 | | |
| 4 | | |
| 5 | LIGHT PEN PRESS | LIGHT PEN TOUCHED TO SCREEN |
| 6 | LIGHT PEN* | CAPTURE BEAM POSITION |
| 7 | +5V | +5 VOLTS POWER (100 mA) |
| 8 | GND | GROUND |
| 9 | | |

## External Disk Connector




| Pin | Name | Description |
|---|---|---|
| 1 | /RDY | Disk Ready—Active Low |
| 2 | /DKRD | Disk Ready Data—Active Low |
| 3-7 | GND | Ground |
| 8 | /MTRXD | Disk Motor Control—Active Low |
| 9 | /SEL2B | Select Drive 2—Active Low |
| 10 | /DRESB | Disk RESET—Active Low |
| 11 | /CHNG | Disk has been Removed from Drive—Latched Low |
| 12 | +5 | 5 VDC Supply |
| 13 | /SIDEB | Select Disk Side—0 = Upper 1 = Lower |
| 14 | /WPRO | Disk is Write Protected—Active Low |
| 15 | /TKO | Drive Head Position over Track O—Active Low |
| 16 | /DKWE | Disk Write Enable—Active Low |
| 17 | /DKWD | Disk Write Data—Active Low |
| 18 | /STEPB | Step the Head—Pulse, First Low then High |
| 19 | DIRB | Select Head Direction—0 = Inner 1 = Outer |
| 20 | /SEL3B | Select Drive 3—Active Low |
| 21 | /SEL1B | Select Drive 1—Active Low |
| 22 | /INDEX | Disk Index Pulse—Active Low |
| 23 | +12 | 12 VDC Supply |

## Power Supply Connector

| Pin | Name |
|---|---|
| 1 | +5Vdc @ 4.3A |
| 2 | SHIELD GROUND |
| 3 | +12Vdc @ 1.0A |
| 4 | SIGNAL GROUND |
| 5 | −12Vdc @ .1A |

## 86-Pin Connector

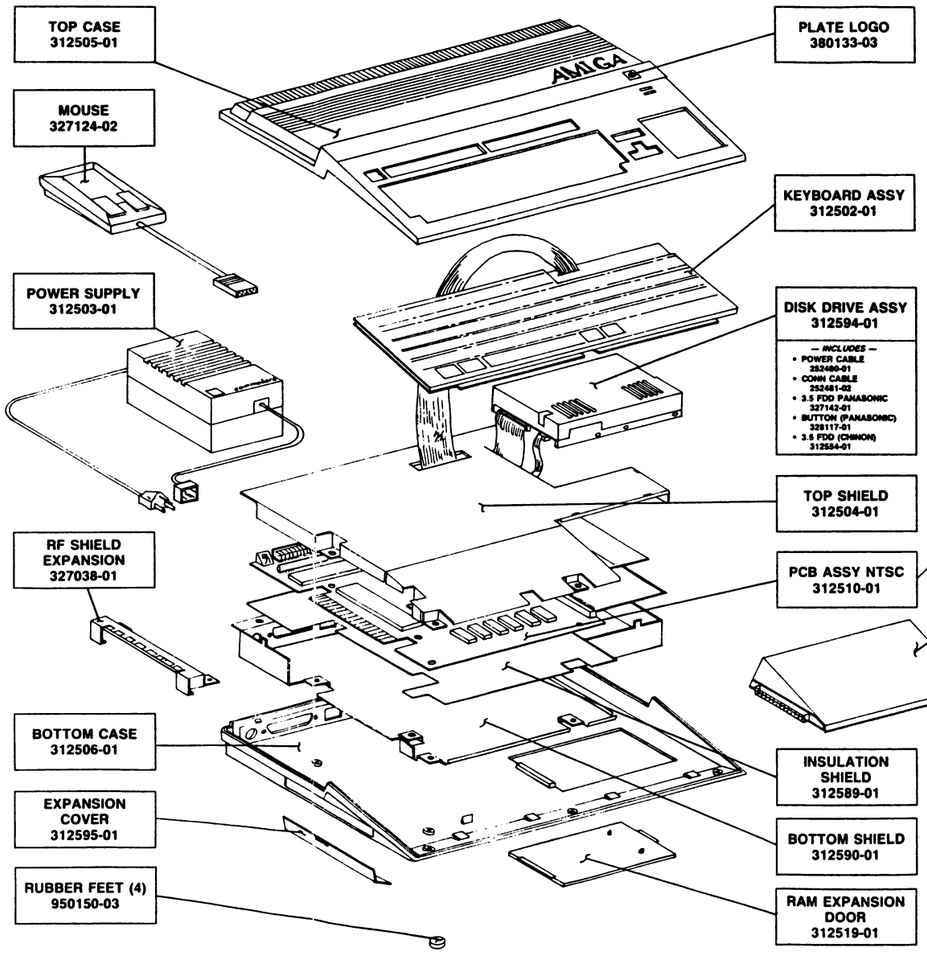
| Pin | Name | Pin | Name |
|---|---|---|---|
| 1 | gnd | 44 | IPL2* |
| 2 | gnd | 45 | A16 |
| 3 | gnd | 46 | BERR* |
| 4 | gnd | 47 | A17 |
| 5 | +5 | 48 | VPA* |
| 6 | +5 | 49 | gnd |
| 7 | exp | 50 | E |
| 8 | −12 | 51 | VMA* |
| 9 | exp | 52 | A18 |
| 10 | +12 | 53 | RES* |
| 11 | exp | 54 | A19 |
| 12 | CONFIG* | 55 | HLT* |
| 13 | gnd | 56 | A20 |
| 14 | C3* | 57 | A22 |
| 15 | CDAC | 58 | A21 |
| 16 | C1* | 59 | A23 |
| 17 | OVR* | 60 | BR* |
| 18 | XRDY | 61 | gnd |
| 19 | INT2* | 62 | BGACK* |
| 20 | PALOPE* | 63 | PD15 |
| 21 | A5 | 64 | BG* |
| 22 | INT6* | 65 | PD14 |
| 23 | A6 | 66 | DTACK* |
| 24 | A4 | 67 | PD13 |
| 25 | gnd | 68 | PRW* |
| 26 | A3 | 69 | PD12 |
| 27 | A2 | 70 | LDS* |
| 28 | A7 | 71 | PD11 |
| 29 | A1 | 72 | UDS* |
| 30 | A8 | 73 | gnd |
| 31 | FC0 | 74 | AS* |
| 32 | A9 | 75 | PD0 |
| 33 | FC1 | 76 | PD10 |
| 34 | A10 | 77 | PD1 |
| 35 | FC2 | 78 | PD9 |
| 36 | A11 | 79 | PD2 |
| 37 | gnd | 80 | PD8 |
| 38 | A12 | 81 | PD3 |
| 39 | A13 | 82 | PD7 |
| 40 | IPL0* | 83 | PD4 |
| 41 | A14 | 84 | PD6 |
| 42 | IPL1* | 85 | gnd |
| 43 | A15 | 86 | PD5 |

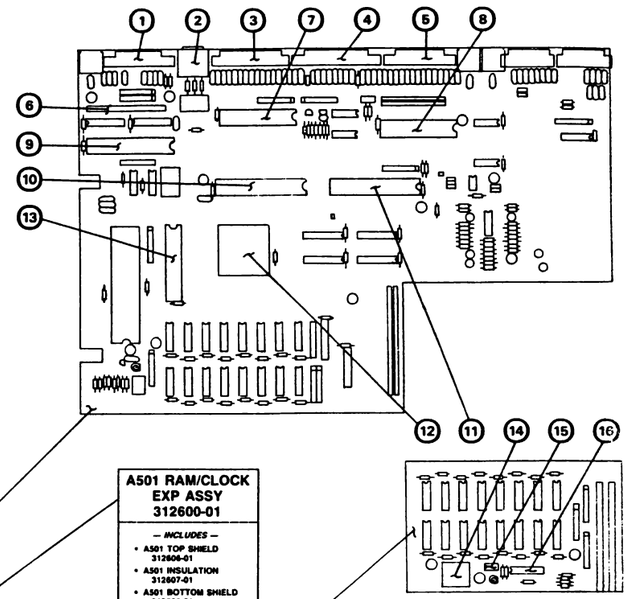
## A500 MAJOR COMPONENT PARTS LIST

| | | |
|---|---|---|
| Power Cable FDD | C | 252480-01 |
| Conn Cable FDD | C | 252481-02 |
| Keyboard Assy — USA/Canada | C | 312502-01 |
| Power Supply | C | 312503-01 |
| Top Shield | C | 312504-01 |
| Top Case | C | 312505-01 |
| Bottom Case | C | 312506-01 |
| PCB Assy — NTSC | C | 312510-01 |
| RAM Expansion Door | C | 312519-01 |
| Floppy Disk Drive (Chinon) | C | 312554-01 |
| Insulation Sheet | C | 312589-01 |
| Bottom Shield | C | 312590-01 |
| Disk Drive Assy | C | 312594-01 |
| Expansion Cover | C | 312595-01 |
| A501 RAM/Clock PCB Assy (With Shields) | C | 312600-01 |
| A501 RAM/CLK PCB Assy (PCB Only) | C | 312604-01 |
| A501 Top Shield | | 312606-01 |
| A501 Insulation Sheet | | 312607-01 |
| A501 Bottom Shield | | 312608-01 |
| Service Manual | C | 314981-01 |
| Users Guide, DOS Manual | C | 317100-01 |
| Amiga Basic Diskette V1.2 | C | 317488-02 |
| Workbench Diskette V1.2 | C | 317608-01 |
| RF Shield Expansion | C | 327038-01 |
| Amiga Basic Manual | C | 327102-01 |
| Mouse | C | 327124-02 |
| Floppy Disk Drive (Panasonic) | C | 327142-01 |
| Button (Panasonic) | C | 328117-01 |
| Plate Logo | C | 380133-03 |
| Rubber Feet | C | 950150-03 |

**C - Indicates Commodore Stocked Part Number**

## SERVICE PARTS REFERENCE DIAGRAM



1. CN9-23P MALE VIDEO - 327032-032
2. CN8-5P SQUARE POWER - 252167-01
3. CN7-25P FEMALE-CENTRONICS - 327033-05
4. CN6-25P MALE - RS232 - 327032-05
5. CN5-23P FEMALE - DISK DRIVE - 327033-03
6. HY1-VIDEO HYBRID - 390229-01
7. 8. U7, U8 - IC8520 R4 - 318029-02
9. U4, IC DENISE 8362 R8 - 252126-01
10. U3, IC PAULA 8364 R7 - 252127-01
11. U5, IC GARY - 318072-01
12. U2, 1C FAT AGNUS 8370 NTSC - 318070-01
13. U6, IC ROM - 315093-01
14. GT1 - BATTERY, NICAD 3.6V 60 WATT - 380393-01
15. Y2 - CRYSTAL 32-768 KHZ - 900560-01
16. U9 - IC REAL TIME CLK OKI MSM6242B - 318073-01

# PARTS LIST

*PCB ASSEMBLY #312510-01*

**PLEASE NOTE:** Commodore part numbers are provided for reference only and do not indicate the availability of parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Approved cross-references for TTL chips, Transistors, etc. are available in manual form through the Service Department, order part #314000-01.

| INTEGRATED CIRCUITS | | |
|---|---|---|
| U1 | MC68000 | 390084-03 |
| U2 | FAT AGNUS 8370 R3 NTSC | 318070-01 |
| U2 | FAT AGNUS 8371 R1 PAL | 318071-01 |
| U3 | PAULA 8364 R7 | 252127-02 |
| U4 | DENISE 8362 R8 | 252126-02 |
| U4 | DENISE 8362 R6 | 252126-01 sub: |
| U5 | GARY 5719 | 318072-01 |
| U7, 8 | 8520R4 | 318029-02 |
| U6 | ROM KICKSTART V1.2 | 315093-01 |
| U16-31 | DRAM 256KX1 150NS | 390026-01 |
| U16-31 | DRAM 256KX1 | 380223-01 sub: |
| U38 | 1488 LINE DRIVER | 901882-01 |
| U39 | 1489 RECEIVER | 901883-01 |
| U14 | LF347/TL084 | 390086-01 |
| U33 | 74F04 | 390110-01 |
| U37 | 74LS32 | 901521-31 |
| U36 | 74LS38 | 901521-38 |
| U32 | 74F74 | 390081-01 |
| U15 | 74LS157 | 901521-11 |
| U34, 35 | 74F244 | 318050-01 |
| U10, 12 | 74LS244 | 901521-13 |
| U40, 41 | 74HC245 | 310003-01 |
| U11, 13 | 74LS373 | 901521-29 |
| U42 | NE555 | 901523-01 |

| TRANSISTORS | | |
|---|---|---|
| Q701 | 2N5770 NPN OSC | 390239-01 |
| Q501, 711 | 2N3904 NPN GP | 902658-01 |
| Q502, 503, 301 | 2N3906 PNP GP | 902707-01 |
| Q321, 331 | JFET MPF 102 | 390252-01 |
| Q321, 331 | JFET PN 4302 | 390254-01 sub: |

| DIODES | | |
|---|---|---|
| D501 | 1N4148 | 900850-01 |

| RESISTORS — All are carbon 1/4 watt, 5% unless noted | | |
|---|---|---|
| RP501 | 10K X9, 10PIN | 902410-18 |
| RP103 | 22 OHM X5 10PIN | 390227-03 |
| RP402, 403 | 47 OHM X4 8PIN | 902422-05 |
| RP201, 202 | 68 OHM X4 8PIN | 902422-06 |
| RP203 | 68 OHM X5 10PIN | 390227-05 |
| RP405 | 120 OHM X5 6PIN | 902441-10 |
| RP104 | 470 OHM X7 8PIN | 902442-17 |

| RESISTORS (Continued) | | |
|---|---|---|
| RP101, 102 401, 501 | 4.7K X9 10PIN | 902410-08 |
| RP404 | 68 OHM X4 8PIN | 902422-06 |
| W1, W2 | ZERO OHM | 390186-01 |
| EMI301, 406 | 1 OHM | 901550-118 |
| EMI401, R405, 406 | 5.1 OHM | 901550-129 |
| R301, 302 | 10 OHM | 901550-64 |
| R101, 102 | 27 OHM | 901550-90 |
| EMI501-503 | 47 OHM 5% ½W | 901600-15 |
| R331, 321 | 360 OHM | 901550-108 |
| R325, 335 | 390 OHM | 901550-57 |
| R305 | 470 OHM | 901550-56 |
| R303, 304, 324, 334, 713, 305 | 1K OHM | 901550-01 |
| R704 | 1.2K OHM | 901550-17 |
| R701 | 2.7K OHM | 901550-23 |
| R702 | 3.9K OHM | 901550-39 |
| R402, 403, 503, 504 | 4.7K OHM | 901550-19 |
| R322, 323, 332, 333, 339, 501, 505, 502, 506 | 10K OHM | 901550-20 |
| R703 | 27K OHM | 901550-15 |
| R712 | 47K OHM | 901550-22 |
| R711 | 1M OHM | 901550-84 |
| R103-108 | 120 OHM | 901550-75 |
| R404 | 120 OHM | 901550-75 |
| R306, 308 | 10K OHM | 901550-20 |
| R307 | 2.7K OHM | 901550-23 |
| R326, 336 | 470K OHM | 901550-82 |
| R409 | 150 OHM | 901550-89 |

| CAPACITORS | | |
|---|---|---|
| C703 | 39pF MLC, AXIAL NPO | 900462-27 |
| C704 | 100pF MLC AXIAL NPO | 900462-37 |
| C705 | 1000pF MLC AXIAL X7R | 900463-16 |
| C411-413, 421-423 | 1000pF MLC AXIAL X7R | 900463-16 |
| C323, 333 | 3900pF MLC AXIAL X7R | 900463-23 |
| C322, 332 | 6800pF MLC AXIAL X7R | 900463-26 |
| C410, 412, 801, 713 | .01μF MLC AXIAL Z5U | 390082-02 |
| C308, 713 | .01μF MLC AXIAL Z5U | 390082-02 |
| C311-314 | .047μF MLC AXIAL X7R | 900463-36 |

# PARTS LIST (continued)

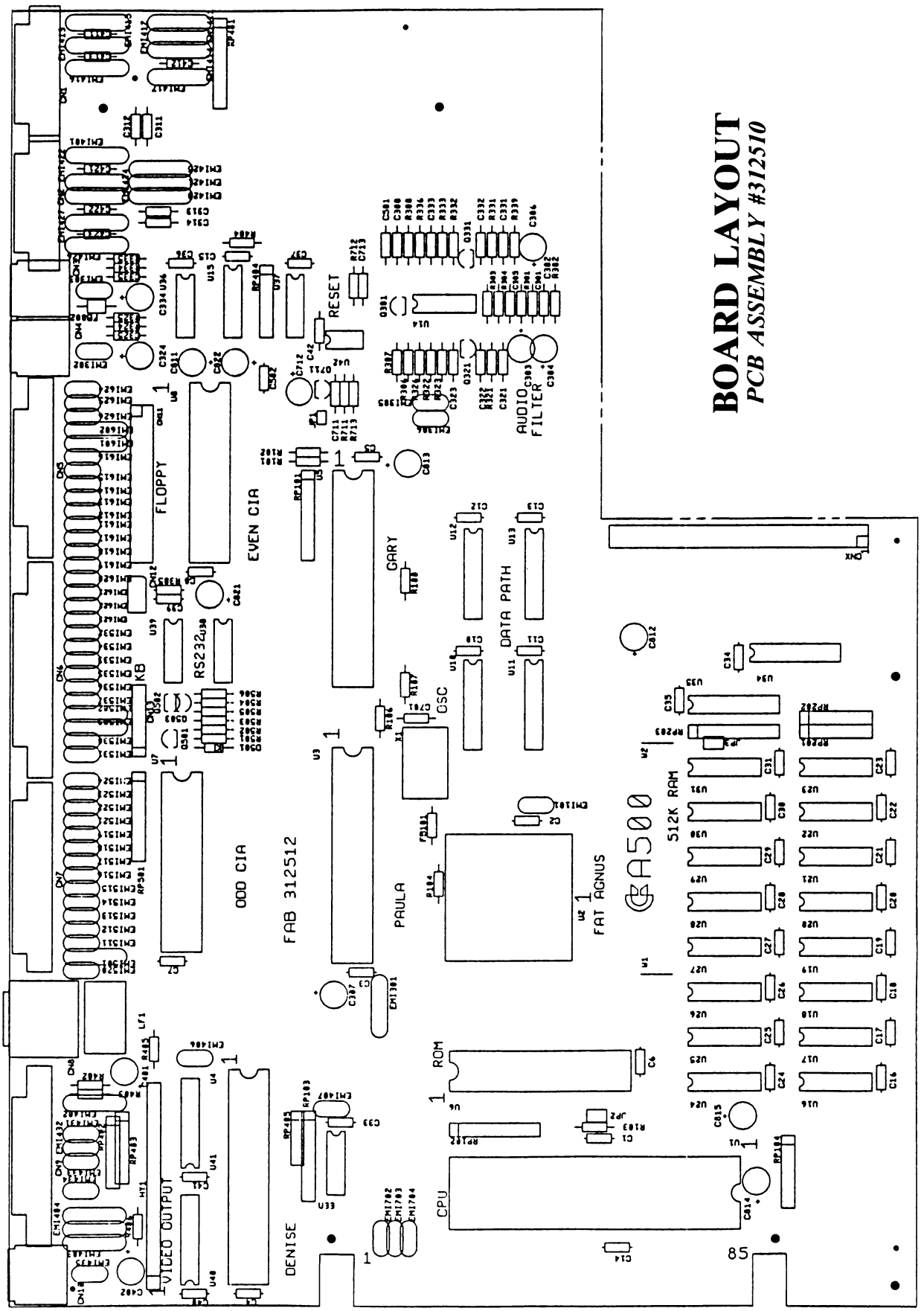
*PCB ASSEMBLY #312510-01*

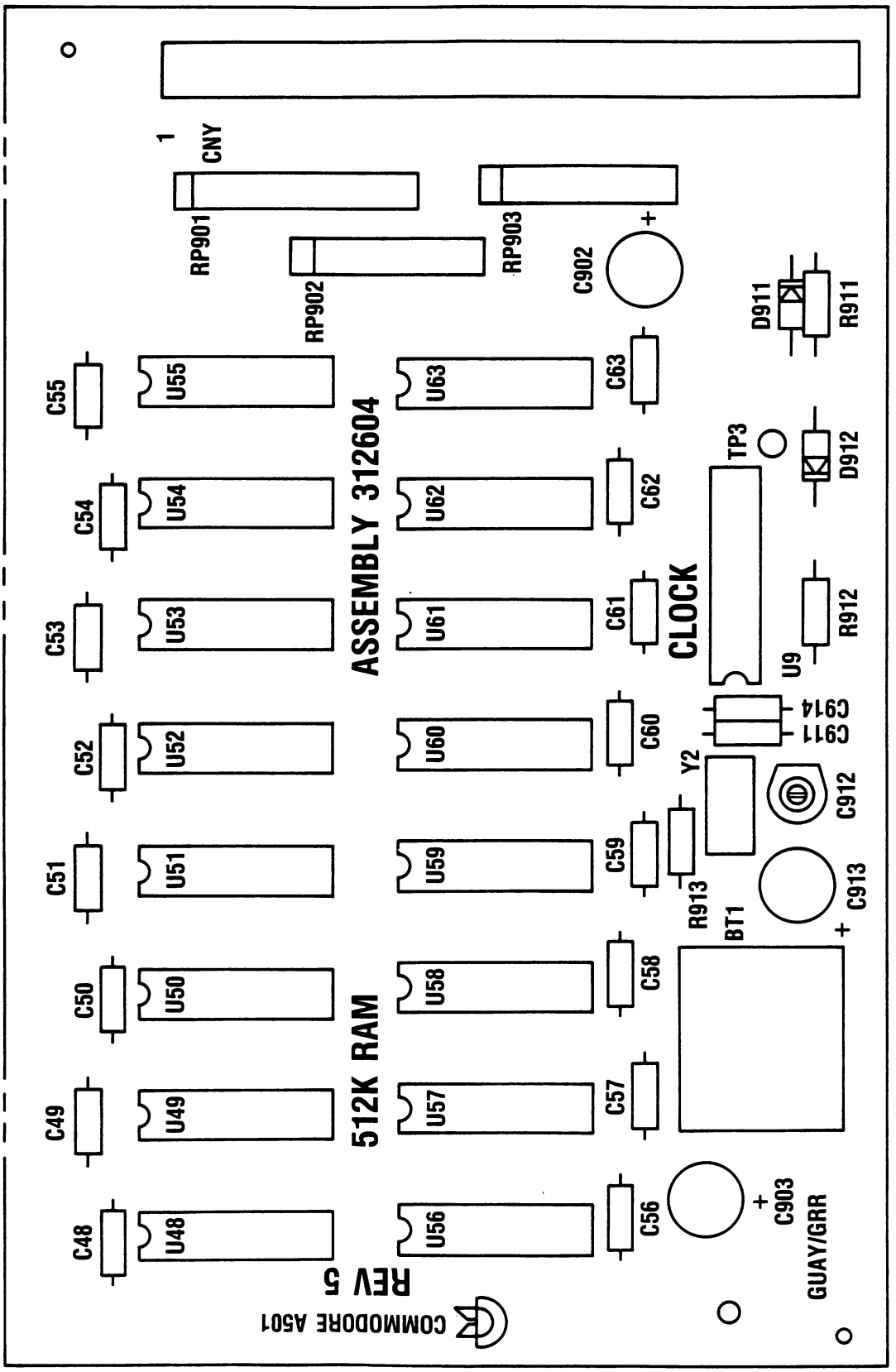
| CAPACITORS (Continued) | | |
|---|---|---|
| C7, 8, 10, 11-13, 15, 33-37, 39, 321, 331, 711, 701 | .1μF MLC AXIAL Z5U | 390082-01 |
| C325, 335 | .22μF MLC AXIAL Z5U | 390082-05 |
| C306, 712 | 10μF ELECT RADIAL | 390101-06 |
| C303, 304, 307, 324 | 22μF ELECT RADIAL | 390101-04 |
| C812-815, 821, 822 | 47μF ELECT RADIAL | 390101-01 |
| C307, 811 | 100μF ELECT RADIAL | 390101-02 |
| C401, 402 | 3300μF 10V ELECT RADIAL | 900100-56 |
| C702 | VARIABLE 4.5-45pF | 251029-06 |
| **MISCELLANEOUS** | | |
| FB802, 101, EMI411-417, 421-427, 402, 431-435 | FERRITE BEAD | 903025-01 |
| EMI302-303, 305, 306, 403-407, 511-524, 531-538, 601, 602, 611-626, 701-704 | EMI FILTER 100pF | 251842-02 |
| HY1 | VIDEO HYBRID | 390229-01 |
| LF1 | LINE FILTER 8 PIN | 251878-02 |
| L701 | CHOKE 3.3μH | 901151-19 |

| MISCELLANEOUS (Continued) | | |
|---|---|---|
| X1 | CRYSTAL 28.63636MHZ NTSC | 325566-14 |
| U6, 7, 8 | SOCKET 40 PIN DIP | 904150-06 |
| U3, 4, 5 | SOCKET 48 PIN DIP | 251313-01 |
| U3, 4, 5 | SOCKET 48 PIN DIP | 251313-02 sub: |
| U2 | SOCKET 84 PIN PLCC | 390185-01 |
| U1 | SOCKET 64 PIN DIP | 904150-10 |
| **CONNECTORS** | | |
| CN8 | DIN 5PIN SQUARE FEMALE - POWER | 252167-01 |
| CN1, 2 | D-SUB 9PIN MALE RA - JOYSTICK | 390242-02 |
| CN9 | D-SUB 23PIN MALE RA - VIDEO | 390242-03 |
| CN5 | D-SUB 23PIN FEMALE RA - DRIVE | 390241-04 |
| CN6 | D-SUB 25PIN MALE RA - RS232 | 390242-06 |
| CN7 | D-SUB 25PIN FEMALE RA - CENTRONICS | 390241-06 |
| CN3 | RCA JACK, WHITE | 252122-01 |
| CN4 | RCA JACK, RED | 252122-02 |
| CN10 | RCA JACK, YELLOW | 252122-03 |
| CN3, 4, 10 | RCA JACK, METAL | 390248-01 sub: |
| CN12 | HEADER 4PIN POLARIZED SIL | 325516-04 |
| CN12 | HEADER 4PIN SIL | 903326-04 sub: |
| CN13 | HEADER 8PIN SIL | 903326-08 |
| CN11 | HEADER 34PIN DIL | 903345-17 |
| CNX | HEADER DUAL RA LONG 56POS MALE | 390243-01 |

# BOARD LAYOUT

*PCB ASSEMBLY #312510*






NOTE: PN #312604-03 — A501 RAM/CLOCK PCB ASSEMBLY — INCLUDES SHIELDS AND INSULATION

## BOARD LAYOUT
## A501 RAM/CLOCK EXPANSION
*PCB ASSEMBLY #312604-03*

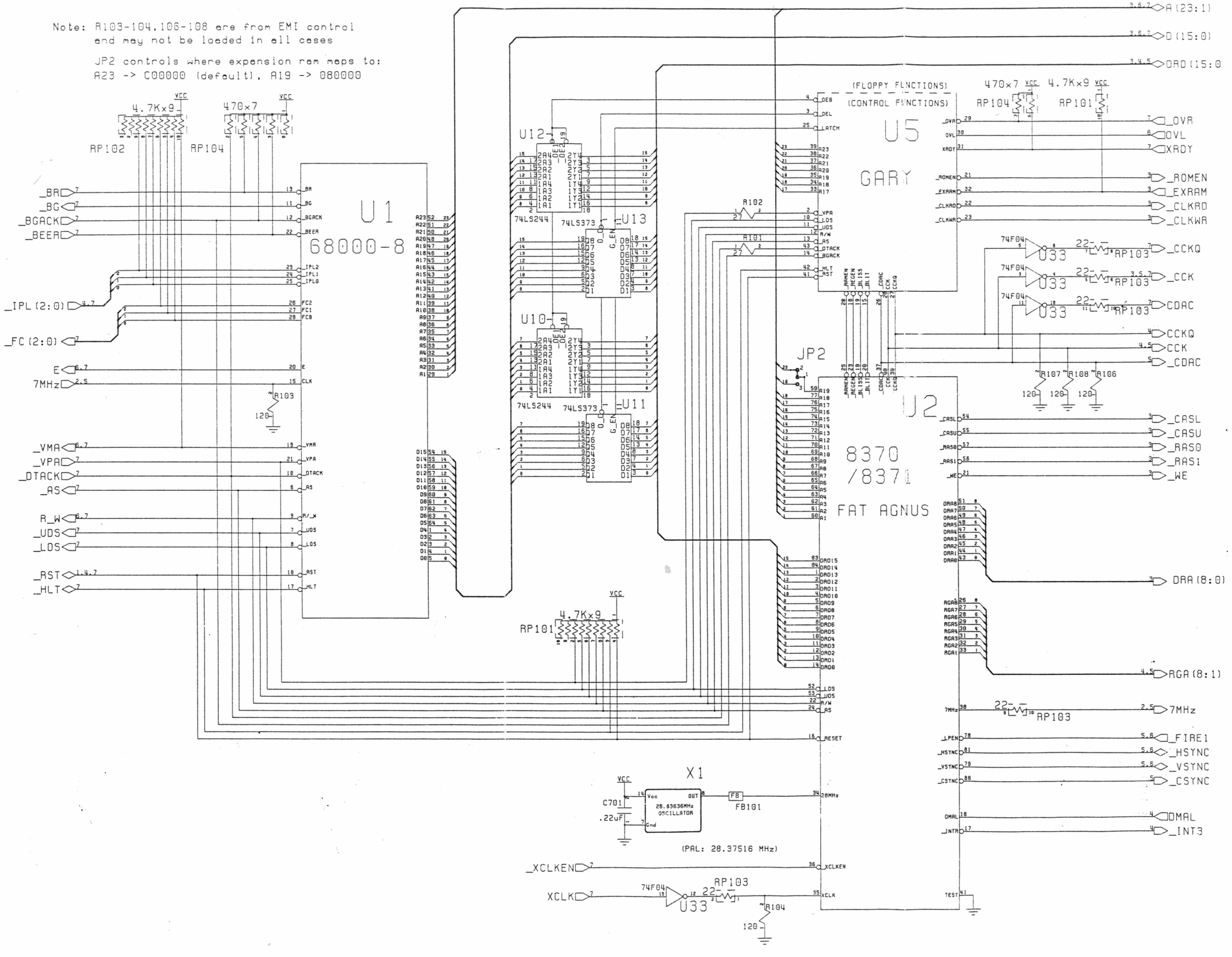
Jumpers and Test Points

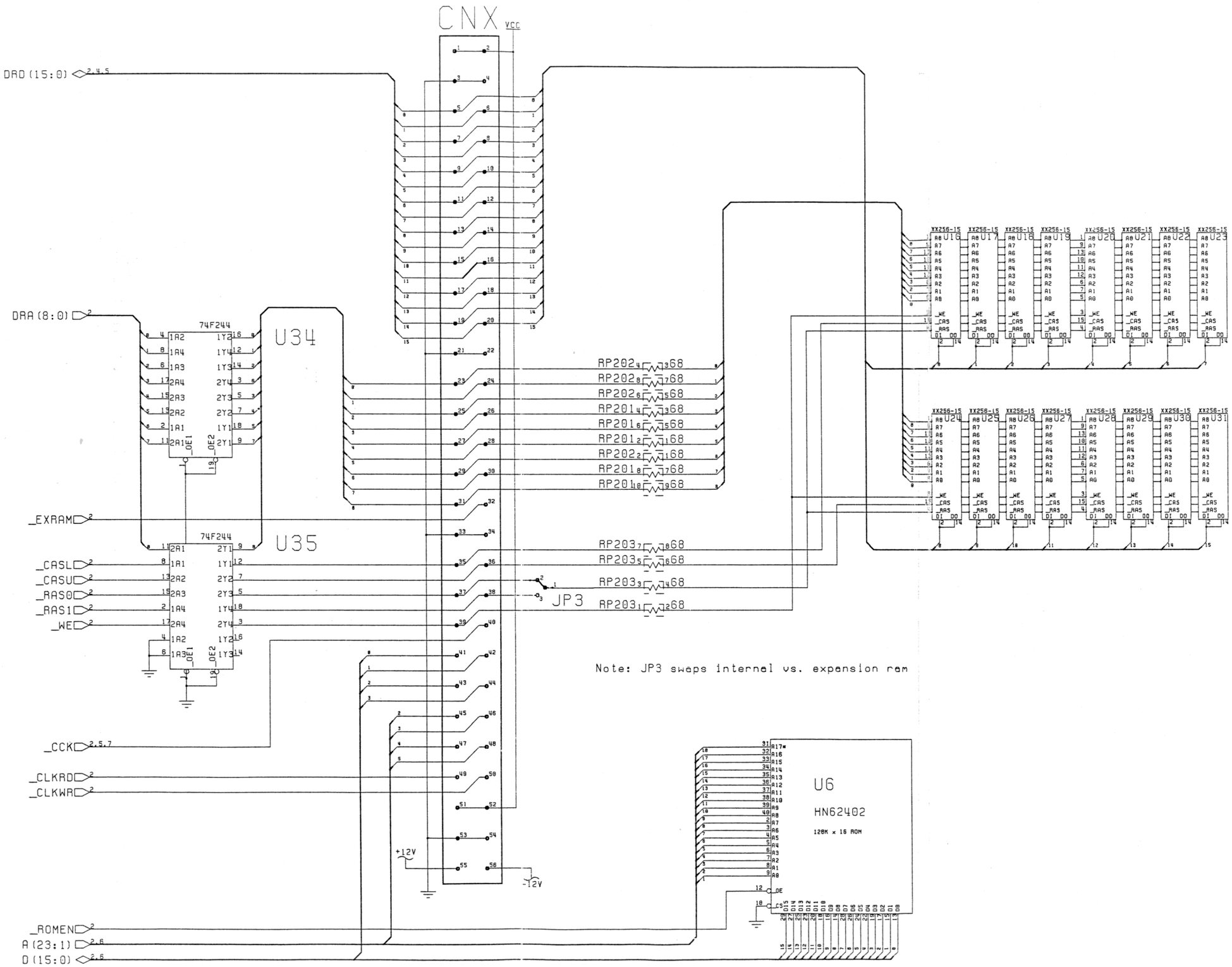
JP1 - System Reset vs. Keyboard Reset
JP2 - Memory Expansion Address Select
JP3 - Internal Memory Address Select

TP1 - 64 Hz Real-Time Clock Test Point

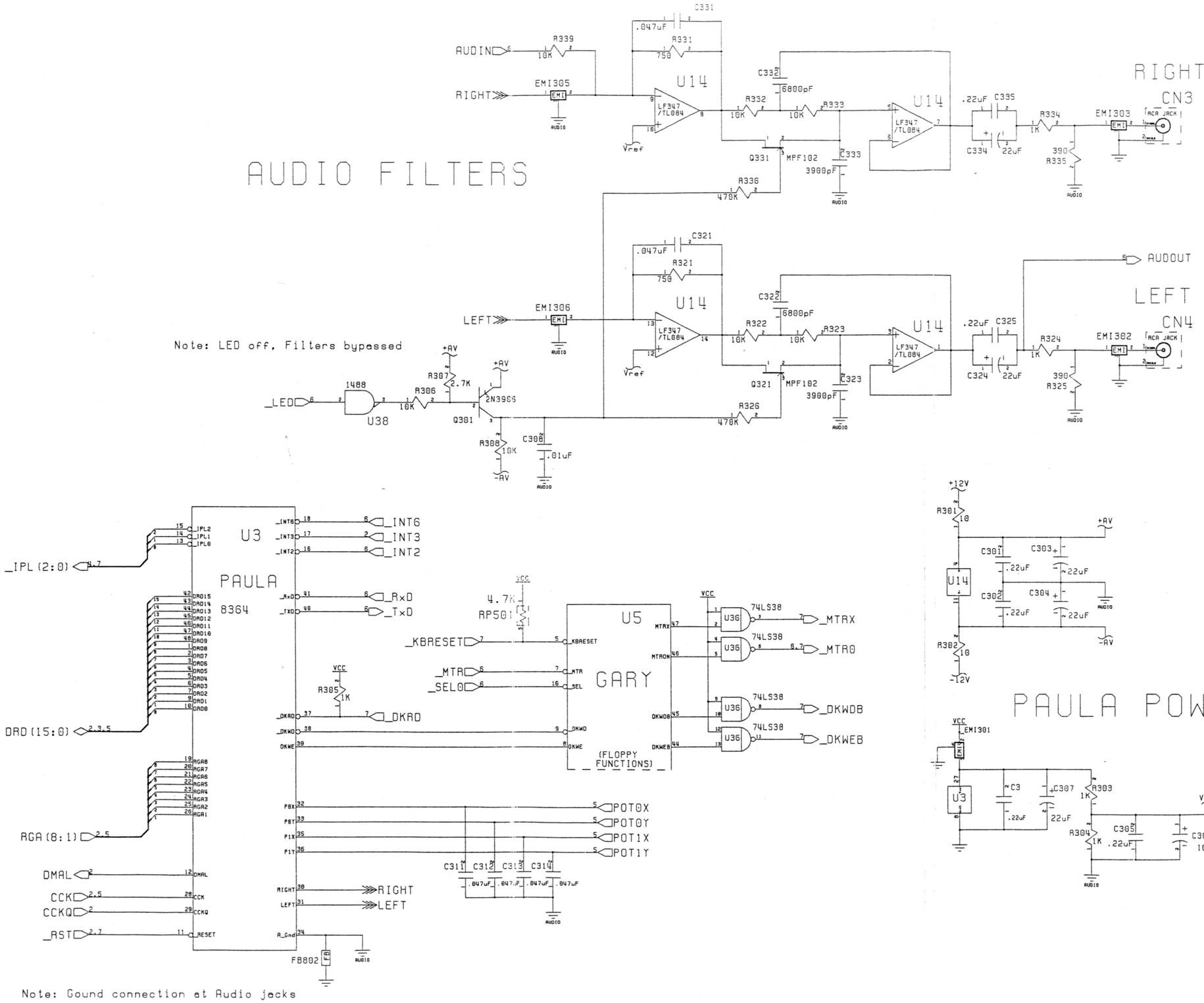
| SIGNAL | DESCRIPTION |
|---|---|
| 28MHZ | 28.63636 MHz Master Clock |
| 7MHZ | 7 MHz Processor Clock |
| A[23:1] | Processor Address (68000) |
| ACK | Data Acknowledge (Parallel) |
| AS | Address Strobe (68000) |
| AUDIN | Audio Input (RS232 jack) |
| AUDOUT | Audio Output (RS232 jack) |
| BEER | Bus Error (68000) |
| BG | Bus Grant (68000) |
| BGACK | Bus Grant Acknowledge (68000) |
| BLISS | Blitter Slowdown (chips) |
| BLIT | Chip Memory Access (chips) |
| BR | Bus Request (68000) |
| BUSY | Device Busy (parallel) |
| CASL/CASU | CAS lower/upper byte (DRAM) |
| CCK | Color Clock aka C1 (chips) |
| CCKQ | Color Clock Quadrature aka C3 (chips) |
| CDAC | 7 MHz Quatrature Clock |
| CHNG | Media Change (floppy) |
| CLKRD/CLKWR | Real-time Clock Read/Write |
| COMP | Composite Monochrome Video (video) |
| CSYNC | Composite Sync (video) |
| CTS | Clear to Send (rs232) |
| D[15:0] | Processor Data (68000) |
| DIR | Direction (floppy) |
| DKRD | Diskette Read Data (floppy) |
| DKWDB | Diskette Write Data (floppy) |
| DKWEB | Diskette Write Enable (floppy) |
| DMAL | Chip DMA Request (chips) |
| DRA[8:0] | DRAM Address (DRAM, chips) |
| DRD[15:0] | DRAM Data (DRAM, chips) |
| DSR | Data Set Ready (rs232) |
| DTACK | Data Transfer Acknowledge (68000) |
| DTR | Data Terminal Ready (rs232) |
| E | Peripheral E Clock (68000) |
| EXRAM | Expansion Memory Present |
| FC[0:0] | Function Control (68000) |
| FIRE0/FIRE1 | Fire Button (joysticks) |
| HLT | Processor Halt (68000) |
| HSYNC | Horizontal Sync (video) |
| INDEX | Diskette Index Hole (floppy) |
| INT[2,3,6] | Interrput Requests (chips) |
| IORESET | I/O Reset |
| IPL[2:0] | Processor Interrupt Requests (68000) |
| KBCLOCK | Keyboard Clock (keyboard) |
| KBDATA | Keyboard Data (keyboard) |
| KBRESET | Keyboard Reset (keyboard) |
| LDS/UDS | Upper/Lower Data Strobe (68000) |
| LED | Power On LED |

| SIGNAL | DESCRIPTION |
|---|---|
| LEFT/RIGHT | Audio Channels |
| MTR | Motor On (floppy) |
| MTR0 | Motor On Drive 0 (floppy) |
| M0V/M0H | Mouse Quadrature Signals (joysticks) |
| M1V/M1H | Mouse Quadrature Signals (joysticks) |
| OVL | Overlay ROM over RAM |
| OVR | Override System Decodeing |
| PIXELSW | Pixel Switch (video) |
| POT0X/POT0Y | Pot Lines (joysticks) |
| POT1X/POT1Y | Pot Lines (joysticks) |
| POUT | Paper Out (parallel) |
| PPD[7:0] | Parallel Port Data (parallel) |
| RAMEN | RAM Enable (chips) |
| REGEN | Chip Register Enable (chips) |
| RAS0/RAS1 | RAS Internal/Expansion Lines (DRAM) |
| RDY | Drive Ready (floppy) |
| RESET | General Reset |
| RGA[8:1] | Register Address Bus (chips) |
| RI | Ring Indicate (rs232) |
| ROMEN | ROM Enable |
| RTS | Request to Send (rs232) |
| RST | Processor Reset (68000) |
| RXD | Receive Data (RS232) |
| RW | Processor Read/Write (68000) |
| SEL | Select (parallel) |
| SEL[3:0] | Drive Select (floppy) |
| SIDE | Side Select (floppy) |
| STEP | Head Step Command (floppy) |
| TRK0 | Track 0 Sense (floppy) |
| TXD | Transmit Data (RS232) |
| VMA | Valid Memory Address (68000) |
| VPA | Valid Peripheral Address (68000) |
| VSYNC | Vertic1 Sync (video) |
| WE | Write Enable (DRAM) |
| WPROT | Write Protect Sense (floppy) |
| XCLK | External 28 MHz Clock (genlock) |
| XCLKEN | External Clock Enable (genlock) |
| XRDY | External Data Ready |


Note: R103-104,106-108 are from EMI control
and may not be loaded in all cases
JP2 controls where expansion ram maps to:
A23 -> C00000 (default), A19 -> 080000
4.7Kx9
470x7
RP102
RP104
U1
68000-8
_BR
_BG
_BGACK
_BEER
_IPL(2:0)
_FC(2:0)
E
7MHz
R103
120
_VMA
_VPA
_DTACK
_AS
R_W
_UDS
_LDS
_RST
_HLT
U12
U13
U10
U11
74LS244
74LS373
RP101
U5
GARY
(FLOPPY FUNCTIONS)
(CONTROL FUNCTIONS)
R102
R101
JP2
U2
8370
/8371
FAT AGNUS
RP104
RP101
_OVR
OVL
XRDY
_ROMEN
_EXRAM
_CLKRD
_CLKWR
74F04
U33
RP103
_CCKQ
_CCK
CDAC
R107
R108
R106
_CASL
_CASU
_RAS0
_RAS1
_WE
DRA(8:0)
RGA(8:1)
7MHz
_FIRE1
_HSYNC
_VSYNC
_CSYNC
DMAL
_INT3
A(23:1)
D(15:0)
DRD(15:0
X1
C701
.22uF
28.63636MHz
OSCILLATOR
FB
FB101
28MHz
(PAL: 28.37516 MHz)
_XCLKEN
XCLK
R104
TEST
RESET


CNX
VCC
DRD(15:0)
DRA(8:0)
74F244
U34
U35
_EXRAM
_CASL
_CASU
_RAS0
_RAS1
_WE
_CCK
_CLKRD
_CLKWR
_ROMEN
A(23:1)
D(15:0)
RP2024 368
RP2028 768
RP2026 568
RP2014 368
RP2016 568
RP2012 168
RP2022 168
RP2018 768
RP2018 968
RP2037 868
RP2035 668
RP2033 468
RP2031 268
JP3
+12V
-12V
XX256-15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
U31
U6
HN62402
128K x 16 ROM
Note: JP3 swaps internal vs. expansion ram

# AUDIO FILTERS



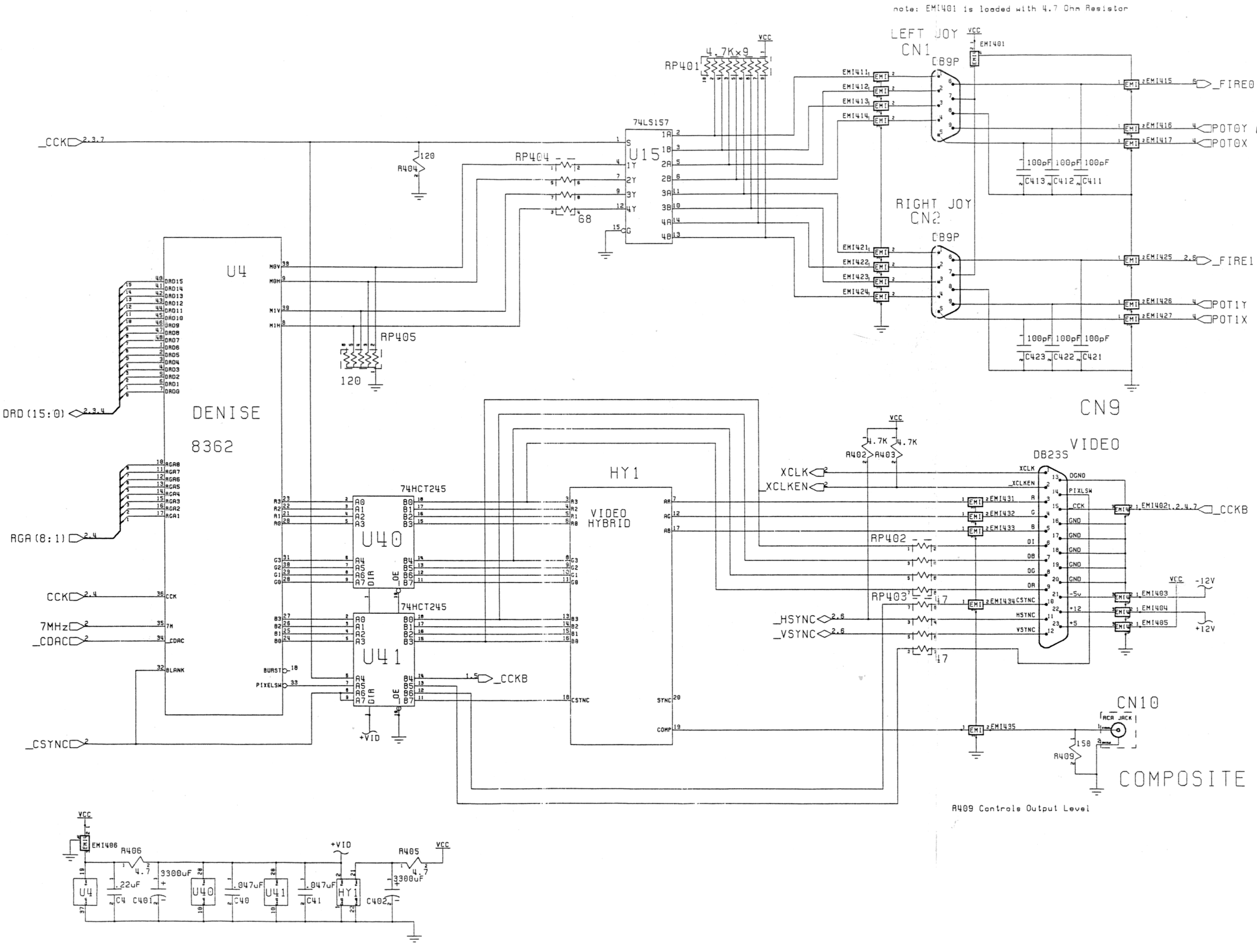


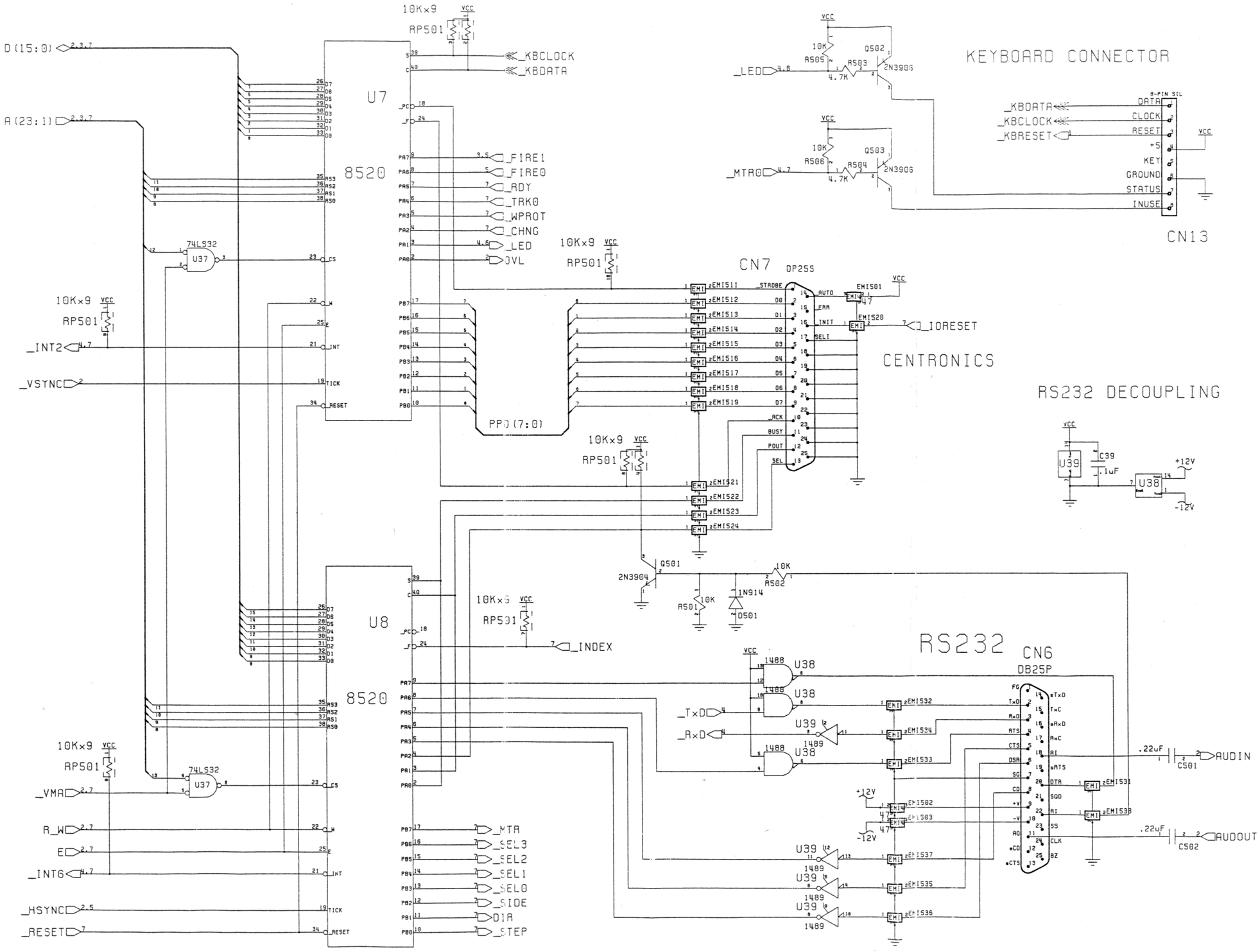


Note: Gound connection at Audio jacks

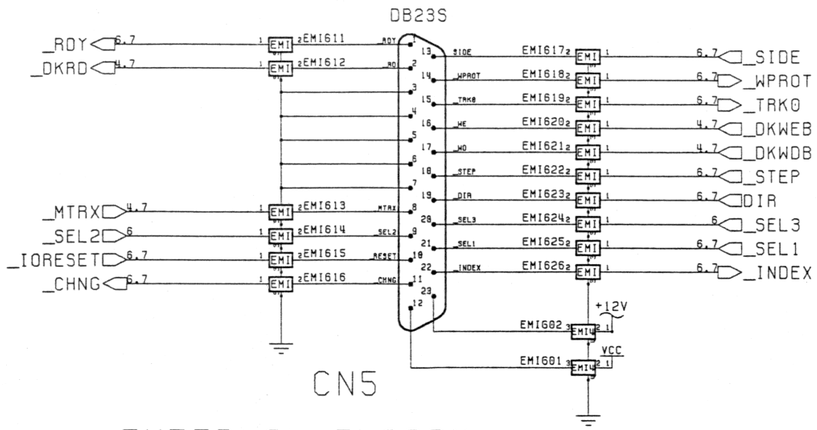


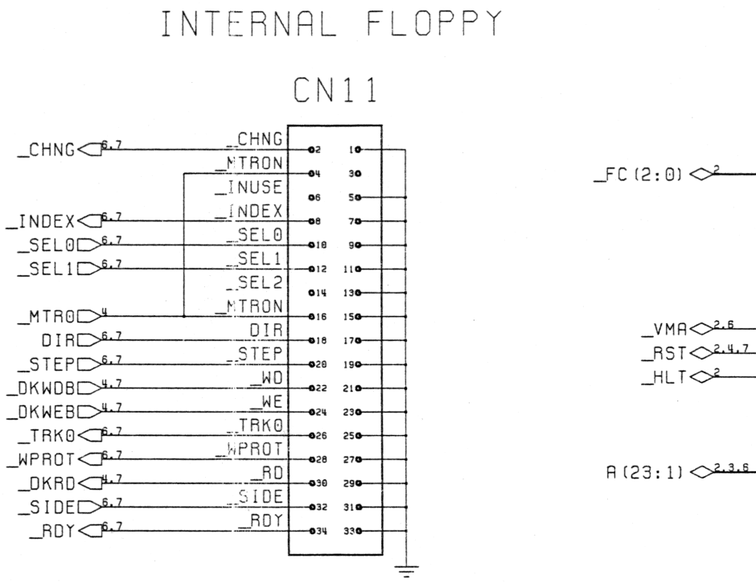

## PAULA POWER!

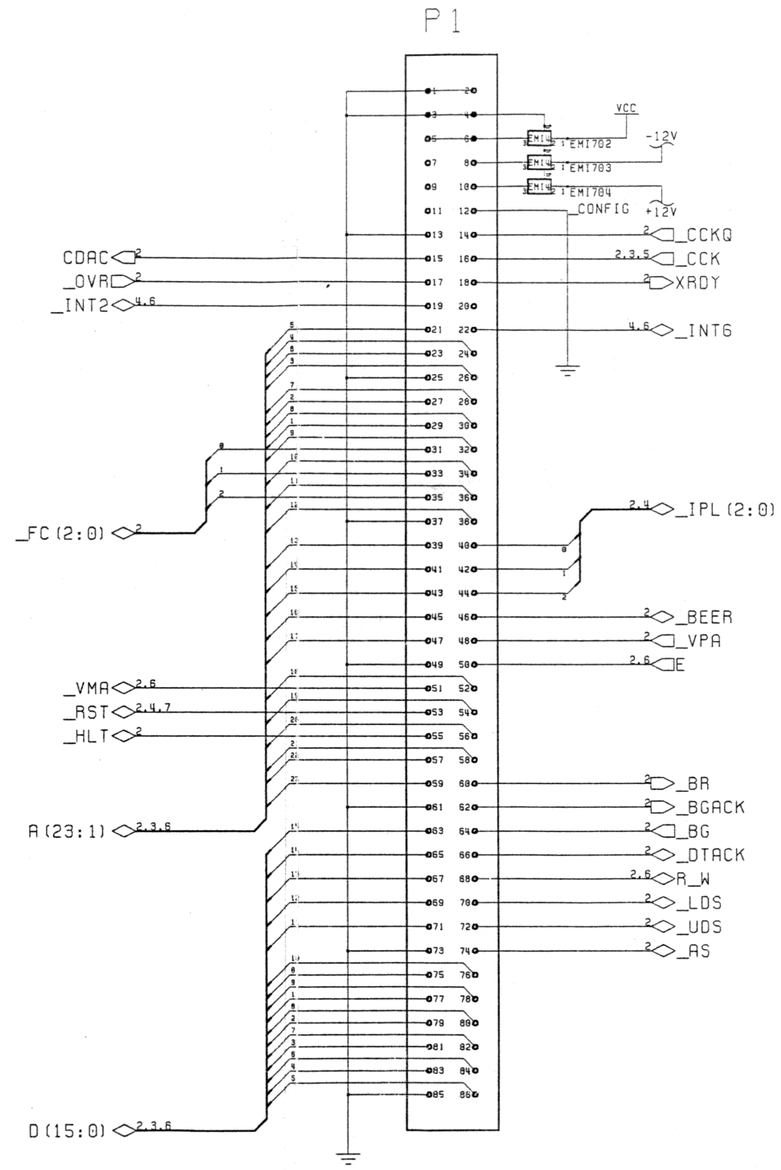

note: EMI401 is loaded with 4.7 Ohm Resistor
LEFT JOY
CN1
DB9P
RIGHT JOY
CN2
DB9P
CN9
VIDEO
DB23S
CN10
RCA JACK
COMPOSITE
74LS157
U15
RP401
4.7Kx9
RP404
68
R404
120
RP405
120
RP402
RP403
4.7K
R402
R403
R406
4.7
R405
4.7
R409
150
U4
DENISE
8362
U40
U41
74HCT245
HY1
VIDEO
HYBRID
DRD(15:0)
RGA(8:1)
_CCK
CCK
7MHz
_CDAC
BLANK
_CSYNC
BURST
PIXELSW
+VID
_CCKB
XCLK
_XCLKEN
_HSYNC
_VSYNC
CSYNC
SYNC
COMP
_FIRE0
POT0Y
POT0X
_FIRE1
POT1Y
POT1X
100pF
C413
C412
C411
C423
C422
C421
.22uF
C4
C401
3300uF
.047uF
C40
C41
C402
VCC
-12V
+12V
+5
-5v
R409 Controls Output Level

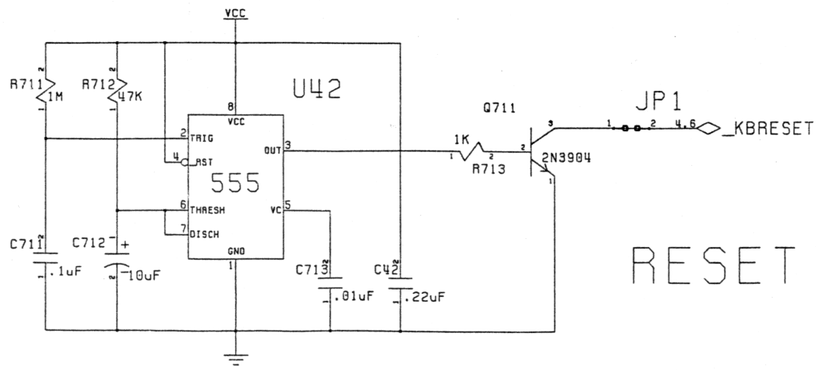


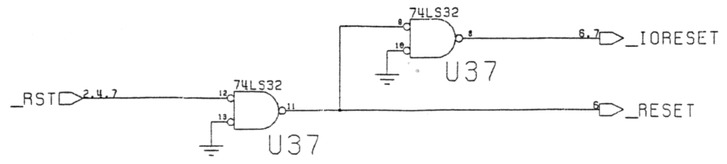

Note: EMI501-503 are loaded with 47 Ohm 1/2 W resistors


DB23S
_RDY
_DKRD
_MTRX
_SEL2
_IORESET
_CHNG
_SIDE
_WPROT
_TRK0
_DKWEB
_DKWDB
_STEP
DIR
_SEL3
_SEL1
_INDEX
+12V
VCC
CN5
EXTERNAL FLOPPY

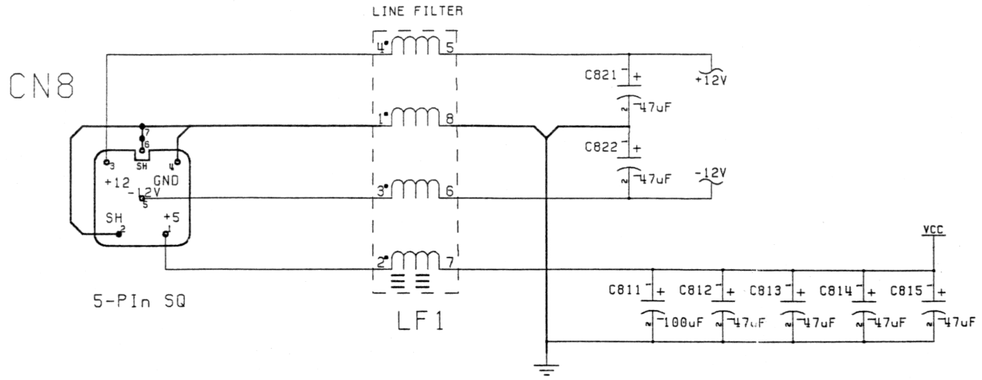

INTERNAL FLOPPY
CN11
_CHNG
_INDEX
_SEL0
_SEL1
_MTR0
DIR
_STEP
_DKWDB
_DKWEB
_TRK0
_WPROT
_DKRD
_SIDE
_RDY


EXPANSION
P1
VCC
-12V
+12V
CONFIG
_CCKQ
_CCK
_XRDY
_INT6
CDAC
_OVR
_INT2
_FC(2:0)
_IPL(2:0)
_VMA
_RST
_HLT
_BEER
_VPA
E
A(23:1)
_BR
_BGACK
_BG
_DTACK
R_W
_LDS
_UDS
_AS
D(15:0)


VCC
U42
555
R711
1M
R712
47K
C711
.1uF
C712
10uF
C713
.01uF
C42
.22uF
Q711
2N3904
1K
R713
JP1
_KBRESET
RESET ACTION

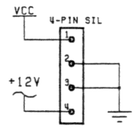

74LS32
U37
_RST
_IORESET
_RESET

# POWER INPUT



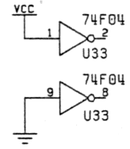

NOTE: HEAVY LINES INDICATE A
SINGLE POINT CONNECTION

# FLOPPY POWER




CN12

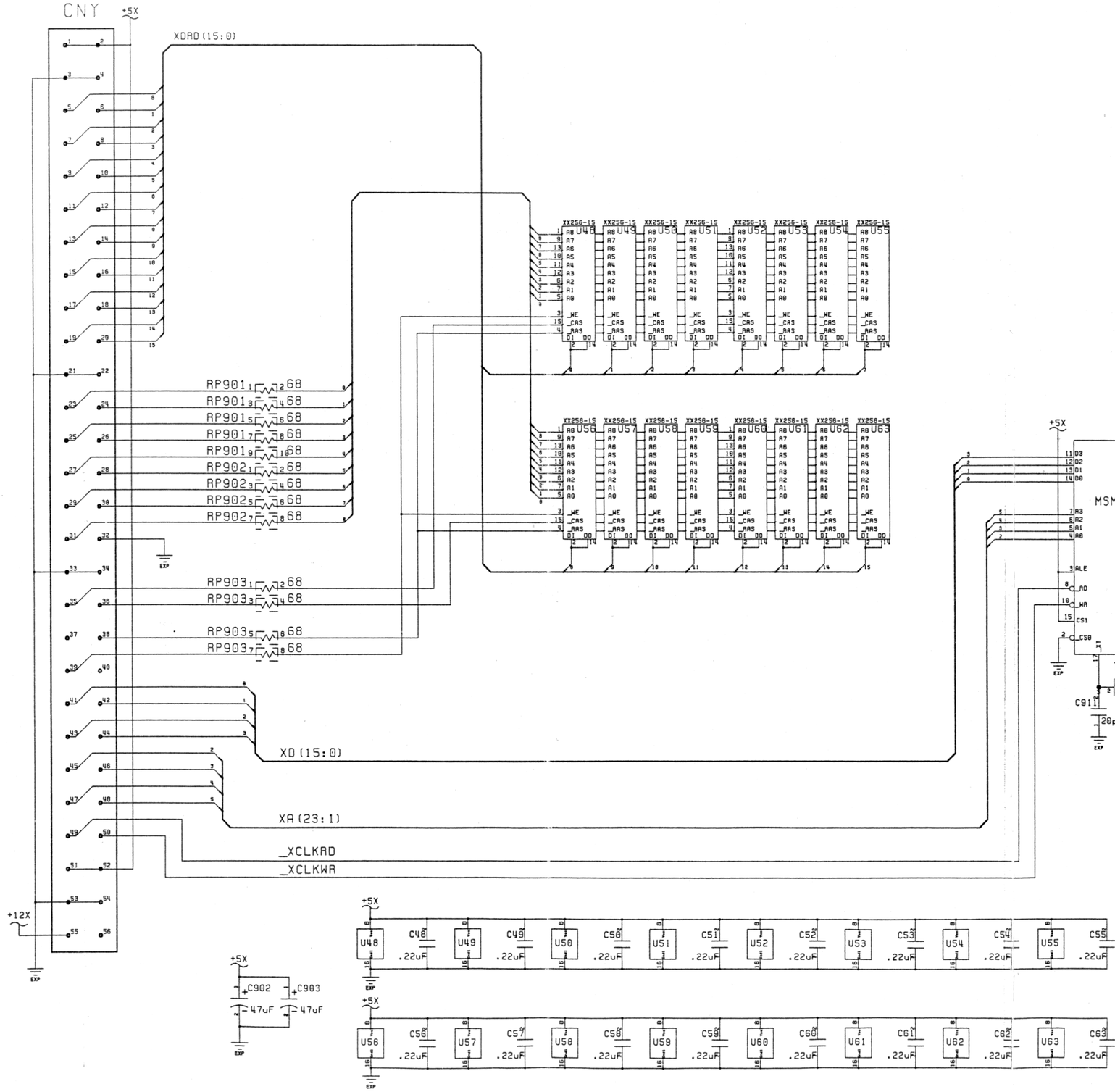
# SPARES







# DECOUPLING


CNY
+5X
XDRD(15:0)
RP901 1 2 68
RP901 3 4 68
RP901 5 6 68
RP901 7 8 68
RP901 9 10 68
RP902 1 2 68
RP902 3 4 68
RP902 5 6 68
RP902 7 8 68
EXP
RP903 1 2 68
RP903 3 4 68
RP903 5 6 68
RP903 7 8 68
XD(15:0)
XA(23:1)
_XCLKRD
_XCLKWR
+12X
U46 U47 U48 U49 U50 U51 U52 U53 U54 U55
U56 U57 U58 U59 U60 U61 U62 U63
XX256-15
A0 A1 A2 A3 A4 A5 A6 A7 A8
_WE _CAS _RAS D1 D0
+5X
C902 47uF
C903 47uF
C48 C49 C50 C51 C52 C53 C54 C55
C56 C57 C58 C59 C60 C61 C62 C63
.22uF
+12X
R911 470
D911 1N914
D912 1N914
R912 10K
TP3
STD.P
R913 470
BT1
3/600K
Ni-Cd
4.5V
180mAH
U9
MSM6242B
D3 D2 D1 D0
R3 R2 R1 R0
ALE
AD
WR
CS1
CS0
VCC
GND
XT
C913 4.7uF
C914 .1uF
Y2
32768Hz
C91 20pF
C912
6.0-45pF

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