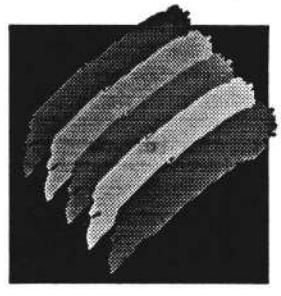
Service Addendum

A4000

AMIGA



Commodore

Section 2 - A4000 Service Addendum
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Chapter 1
Introduction

The *A4000 Service Addendum* supplements the *A4000 User's Guide*. This addendum provides the following information:

- Listing of general system features
- Pointers to specific information about the system
- Explanation of the POST test diagnostics
- Jumper settings not described in the *A4000 User's Guide*
- Instructions for replacing the motherboard and power supply
- Bill of Materials
- System specifications
- System schematics

System Features

The Amiga 4000 (A4000) offers the most advanced set of features in the Amiga line. These features include:

- Motorola 68040/30 series microprocessor running at 25 MHz, on a removable processor module
- AA custom chipset offering graphics with 256 colors from a palette of 16.8 million in all color modes
- Up to 2 MB 32-bit "Chip" memory using SIMMs
- Up to 16 MB 32-bit "Fast" memory using SIMMs
- Four Zorro III AUTOCONFIG expansion slots
- Extended video slot
- Local-bus CPU slot
- Three PC/AT compatible bridge shots
- High-capacity (1.76 MB) floppy drive
- AT IDE hard disk drive interface (16-bit)
- Mounting provisions for internal 3.5-inch and 5.25-inch devices
- Four-voice stereo sound output
- Front panel keylock for security

See Appendix A of the *A4000 User's Guide* for a complete listing of the system's technical specifications.

A4000 User's Guide

This guide acquaints you with the system and offers instruction for system upgrades. It also tells you what information a user has at his disposal. The guide includes the following information:

- Locating system features (Chapter 1)
- Booting the system (Chapter 2)
- Opening the system case (Chapter 3)
- Identifying internal components (Chapter 3)
- Identifying motherboard expansion options (Chapter 4)
- Installing motherboard expansion options (Chapter 4)
- Installing expansion boards (Chapter 5)
- Identifying internal storage bays (Chapter 6)
- Installing internal storage devices (Chapter 6)
- Identifying system problems (Chapter 7)
- Listing technical specifications (Appendix A)
- Listing pin assignments for input/output connectors (Appendix B)
- Using floppy disks (Appendix C)
- Motherboard layout (Appendix D)

Chapter 2
Diagnostics

There are two types of diagnostic tools available for the A4000:

System Startup	Built into the ROM to run automatically when the system is turned on
Third party diagnostics	Memory and port tests available from third party vendors

System Startup

The system startup sequence consists of a series of tests that run automatically whenever you turn on the computer. This test series resides permanently in the BIOS. It performs CPU and keyboard tests to verify basic system operations.

If the system finds an error before the screen display turns on, the screen will remain blank and the system halts. After the screen display turns on, the screen changes color and the system halts if an error occurs. The screen color helps you identify the type of system problem. The screen colors represent:

Test Status	Color	Description
Passed Test	Light Gray	Initial hardware configuration tests passed
		Initial system software tests passed
		Final initialization test passed
Failed Test	Red	ROM error - Reseat or replace
	Green	Chip RAM error (reset AGNUS and re-test)
	Blue	Custom Chip(s) error
	Yellow	68000 detected error before software trapped it (GURU)

The system performs the following test sequence:

1. Delays beginning the tests a fraction of a second to allow the hardware to stabilize.
2. Jumps to ROM code in diagnostic card (if found).
3. Disables and clears all DMA and interrupts.
4. Turns on the screen.
5. Checks the general hardware configuration.

   If the screen remains a light gray color and the tests continue, the hardware is O.K.

   If an error occurs, the system halts.
6. Performs checksum test on ROMs.

   If the system fails the ROM test, the screen display turns red and the system halts.

7. Begins the system startup sequence.
8. Sets up temporary exception processing.

   If a processor error occurs, the screen display turns yellow and the system halts.
9. Tests the Chip RAM.

   If memory configuration error occurs, the screen display turns green and the system halts.
10. Tests Custom IC register addresses.

    If address error occurs, the screen display turns blue and the system halts.
11. Checks to see if the system software is operating properly.
12. Restores screen.

Third Party Diagnostics

There are several third-party diagnostic programs available that test additional system functionality. Although Commodore cannot guarantee their accuracy in performance and will in no way be responsible for system damage resulting from their use, you may find them helpful in identifying system problems.

Memory

The MBRTest-2 utility, designed by MicroBotics, Inc. runs memory tests under AmigaDOS 1.3, 2.0 and 3.0. It tests all memory types on the motherboard and the bus. For information contact:

MicroBotics, Inc.
1251 American Parkway
Richardson, Texas 75081
USA
Telephone (214) 437-5330

Ports

The ProPort Analyzer for the Amiga utility tests the game, parallel, serial, video, audio ports plus disks and memory. For more information contact:

Amazing Computer
1441 East Flecher Avenue
Tampa, Florida 33612
USA
Telephone (813) 977-6511

Chapter 3

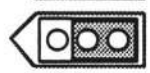
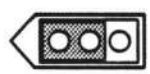
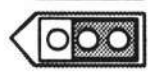
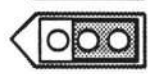
Jumpers

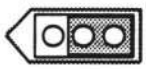
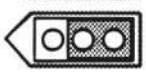
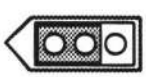
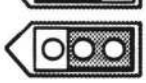
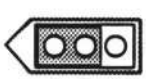
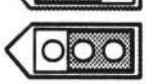
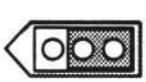
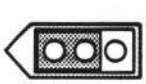
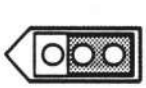
Setting a Jumper

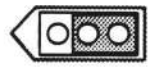
1. Determine the jumper(s) you want to verify or change by looking at the function column of the jumper tables in this chapter.
2. Remove the system cover. Refer to Chapter 3 of the *A4000 User's Guide* for instructions.
3. Locate the jumper(s) on the motherboard or processor board. Use the drawings in this chapter as you look at the actual board.
4. Verify or reset the jumper(s) according to the diagram in the jumper table in this chapter.

Motherboard Jumpers

This table provides the settings for the motherboard jumpers. An asterisk (*) in the jumper column marks the two jumpers that can be changed by the user. A double asterisk (**) in the jumper column indicates that the jumper setting is dependent on the hardware configuration of the system.

Function	Jumper	Setting	Description
CLK90 Clock Source**	J100:1-2 closed		Internal (020/030)
	J100:2-3 closed		External (040)
CPU Clock Source**	J104:1-2 closed		Internal
	J104:2-3 closed		External
ROM Speed	J151:1-2 closed		200 ns
	J151:2-3 closed		160 ns

Function (cont'd)	Jumper (cont'd)	Setting (cont'd)	Description (cont'd)
Chip RAM Size	J213:1-2 closed		2 MB
	J213:2-3 closed		8 MB (not supported)
Enable Second Internal Floppy Drive*	J351:1-2 open		No second internal floppy drive, or 1.76 MB floppy drive as DF1:
	J351:1-2 closed		Enable second internal floppy drive (880 KB) as DF1:
Redirect DF0:	J352:1-2 closed		Internal: DF0: and DF1: internal DF2: and DF3: external
	J352:2-3 closed		External: DF2: and DF1: internal DF0: and DF3: external
Enable DSACK (when CPU is 68020)	J850:1-2 closed		DSACK enable. Required if CPU is a 68020. Also requires U860 and U152.
	J850:1-2 open		No DSACK
RAM Size	J852:1-2 closed		RAM size 1 MB x 32
	J852:2-3 closed		RAM size 256 KB x 32
Select NTSC/PAL	J212:1-2 closed		Select NTSC
	J212:2-3 closed		Select PAL
VBB\MA10	J214:2-3 closed		Supplies VBB to ALICE
	J214:1-2 closed		ALICE supplies MA10 for 8 MB chip RAM (not supported)
Select Sync on Green	J500:1-2 closed		Sync on green disabled
	J500:2-3 closed		Sync on green enabled
LISA Sync	J501:2-3 closed		Default

Function (cont'd)	Jumper (cont'd)	Setting (cont'd)	Description (cont'd)
Select DAC Sync	J502:1-2 closed		DAC syncs on green
	J502:2-3 closed		DAC used standard signal

Motherboard Jumper Locations

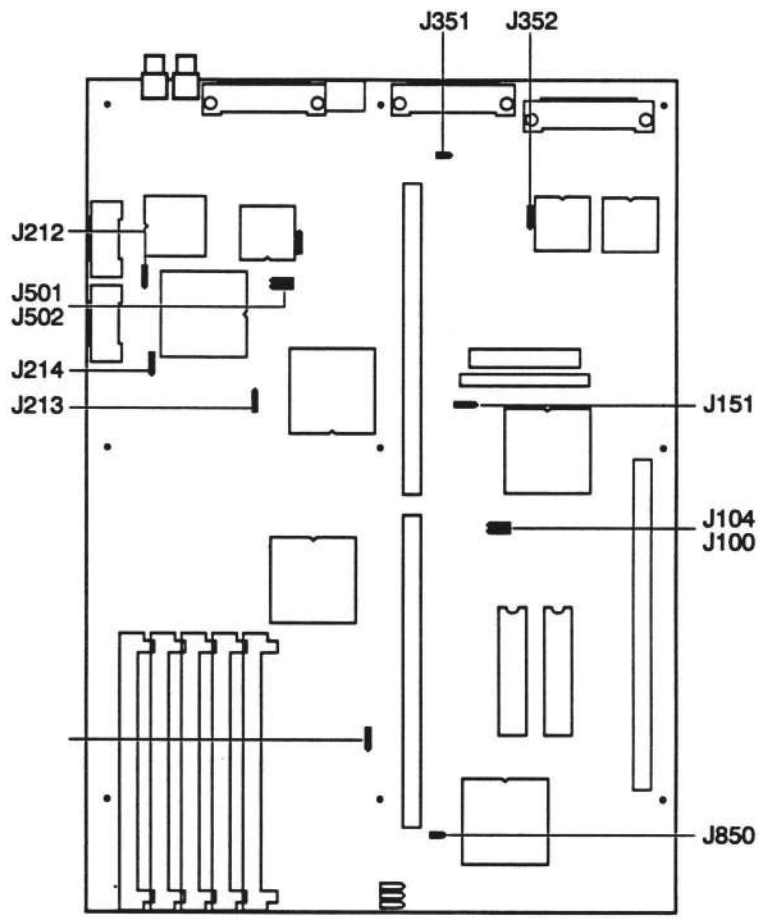
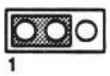
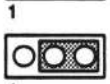
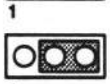
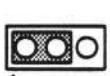
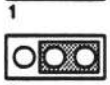


Figure 3-1. Motherboard Jumper Locations

68020/68030 and EC030 Processor Card Jumpers

Function	Jumper	Setting	Description
FPU Select PLCC/PGA	J100:1-2 closed	 1	Use FPU in PLCC location
	J100:2-3 closed	 1	Use FPU in PGA location
FPU Clock	J100:1-2 closed	 1	Use optional on-board oscillator (U103)
	J100:2-3 closed	 1	Use CPU clock
MAPROM Enable (requires U100)	J103:1-2 closed	 1	MAPROM disabled
	J103:2-3 closed	 1	MAPROM enabled
68020 Selected	J201:1-2 closed	 1	68020 not selected
	J201:2-3 closed	 1	68020 selected
68030 Selected	J202:1-2 closed	 1	68030 selected
	J202:2-3 closed	 1	68030 not selected
020/030 Select	J203:1-2 closed	 1	68030 selected
	J203:2-3 closed	 1	68020 selected

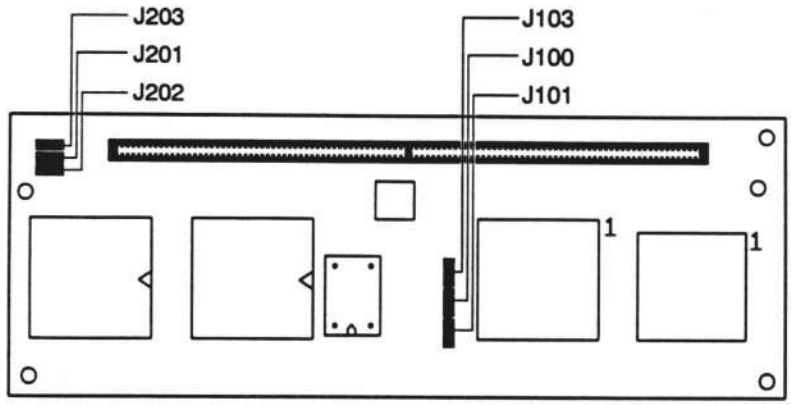


Figure 3-2. 68020/68030 Processor Card Jumper Locations

68040 Processor Card Jumpers

Function	Jumper	Setting	Description
Enable *CDIS *MDIS	J100:1-2 closed		Enable CDIS* MDIS*
	J100:3-4 closed		Enable CDIS* MDIS* (close both sets of jumpers)
Enable MAPROM	J400:1-2 closed		MAPROM enabled
	J400:2-3 closed		MAPROM disabled
Test	TJ100:1-2 closed		Test jumper

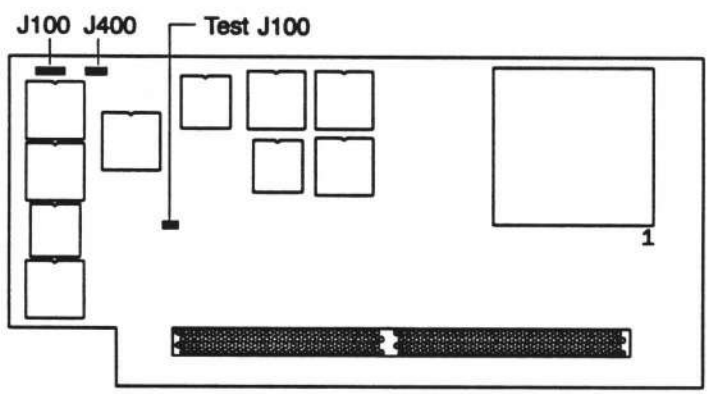


Figure 3-3. 68040 Processor Card Jumper Locations

Chapter 4

Replacing the Motherboard and Power Supply

The chapter provides instructions for removing and replacing the system motherboard and power supply. Refer to the *A4000 User's Guide* for information on installing motherboard options, expansion boards and optional storage devices.

Replacing the Motherboard

Follow these instructions to remove and replace the motherboard.

1. Remove the A4000 system cover. See Chapter 3 in the *A4000 User's Guide* for instructions.
2. Remove the front panel. Use Figure 4-1 to locate the plastic clips located inside the system's front panel. The location is shown on the outside of the front panel, but the clips are attached to the panel's interior. Use needle nosed tweezers to squeeze the clips and pry them out of the system chassis. Pry the top three clips out first, then pry a lower corner clip out of the chassis. Move the front panel gently away from the system chassis.

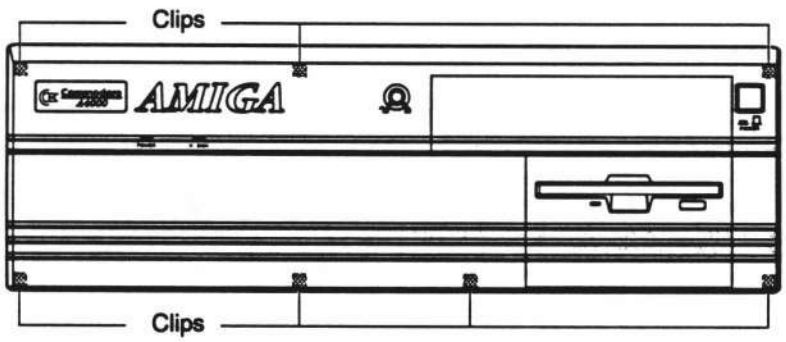


Figure 4-1. Front Panel Clip Locations

3. Remove the front drive bay bracket and installed drives (such as CD-ROM, floppy or tape). See Chapter 6 in the *A4000 User's Guide* for instructions.
4. Remove the hard disk bracket and drive. See Chapter 6 in the *A4000 User's Guide* for instructions.
5. Remove any expansion boards installed in the daughterboard. See Chapter 5 in the *A4000 User's Guide* for instructions.
6. Remove the daughterboard bracket. Locate the bracket screws in Figure 4-2. Remove the two screws and detach the daughterboard bracket from the system chassis.

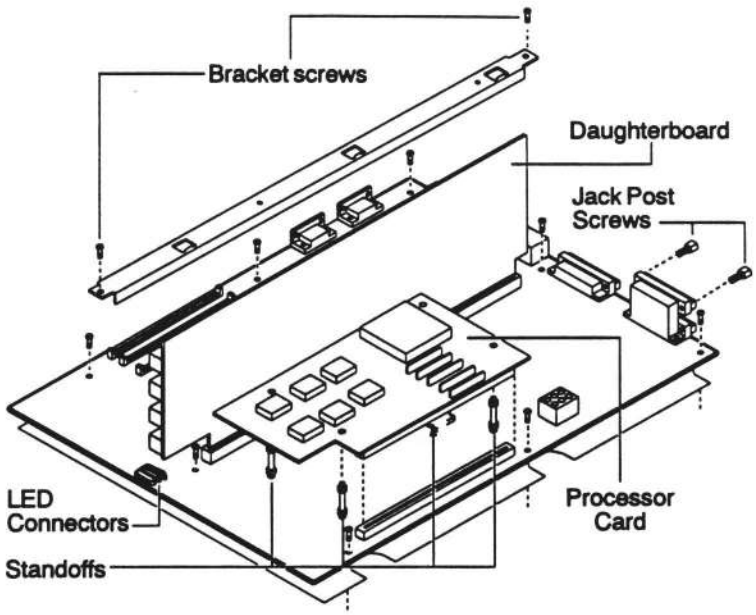


Figure 4-2. Daughterboard Top Bracket

7. Remove the daughterboard by gently pulling the board from its motherboard socket.
8. Remove the processor board. Locate the standoffs attaching the processor board to the motherboard in Figure 4-2. Use needle nose tweezers to squeeze each standoff as you gently pull the processor board upward to release it from the motherboard. The standoffs will pop back into place when you replace the processor board.
9. Remove the expansion bracket. Locate the expansion bracket screw in Figure 4-3. Remove the screw and the bracket.

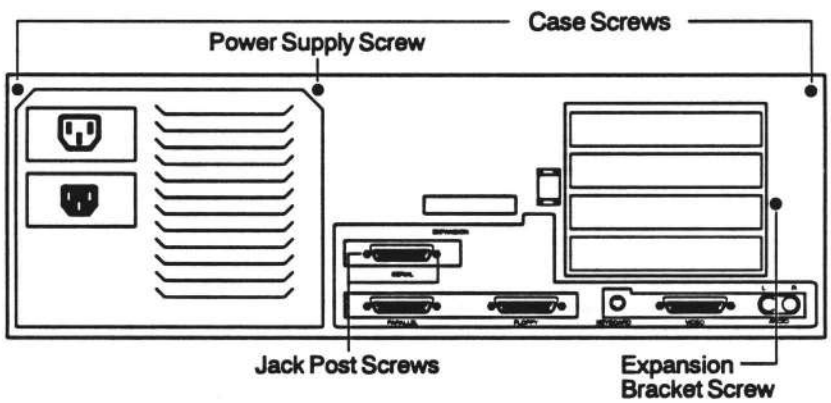


Figure 4-3. Jack Post and Expansion Bracket Screws Location

10. Remove the jack post screws. Locate the jack post screws attaching the motherboard to the chassis in Figure 4-2 and remove the two screws.
11. Remove the hard disk (red wire), power (white wire) and key switch (blue wire) LEDs connecting the motherboard to the front panel.

12. Remove motherboard from the chassis. Locate the screws attaching the motherboard to the chassis in Figure 4-4. Remove the screws and the motherboard.

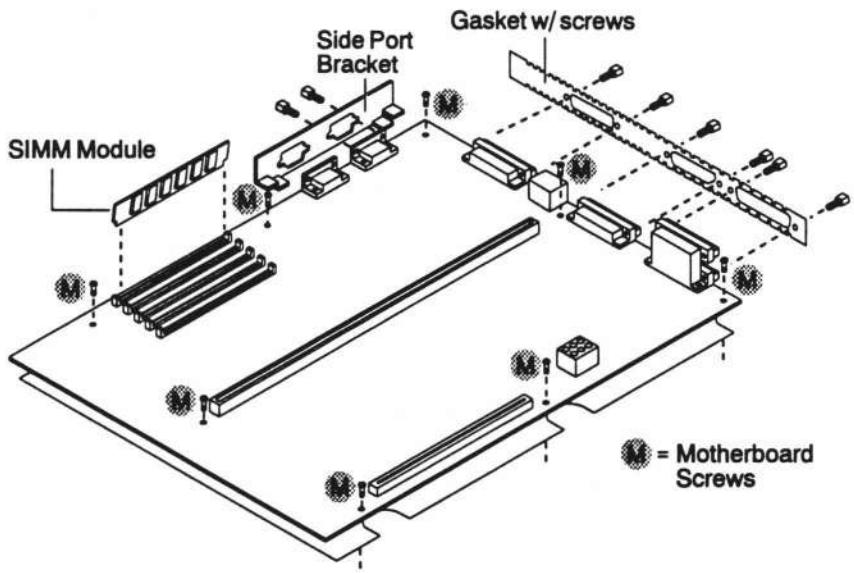


Figure 4-4. Motherboard Chassis, Expansion Bracket

To replace the motherboard reverse the steps you followed to remove the board.

If you are replacing the motherboard with a new motherboard, the new board may not have a side port bracket or a gasket. If they are not on the new board, follow these steps:

1. Locate the side port bracket and gasket in Figure 4-4.
2. Remove the screws and the side port bracket and gasket from the motherboard.
3. Reattach them to the new motherboard before installing it in the system chassis.

Replacing the Power Supply

Follow these instructions to remove and replace the power supply.

1. Follow steps 1-4 in the list describing removing the motherboard.
2. Locate the power supply button in Figure 4-5 and pull it out of the power supply.
3. Locate the power supply screw attaching the power supply to the system chassis in Figure 4-3 and remove the screw.
4. Remove the power supply by sliding it forward and upward as illustrated in Figure 4-5.

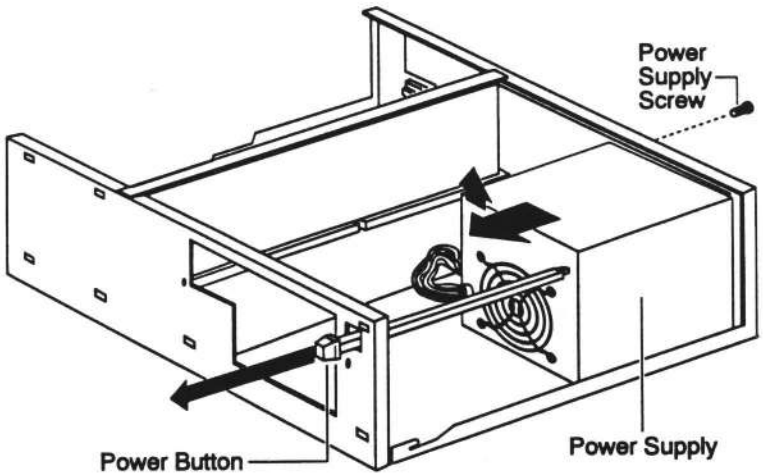


Figure 4-5. Power Supply

To replace the power supply reverse the steps listed above. Make certain the tabs on the bottom of the power supply case fit into the grooves on the system chassis.

Chapter 5
Bill of Materials

The following information is taken from the A4000 Bill of Materials (BOM).

- Title of the drawing
- Number and revision level of the drawing
- Part number of each part
- Description of each part
- Reference description/notes for each part

The BOM contains additional product configuration data not reproduced in this table. The BOM is updated from time-to time. For a complete current listing of all the information contained in a BOM (including line item numbers), request the latest revision BOM drawings by drawing number from Engineering Documentation in West Chester.

LED Assembly, Power On (363772 Rev 4)

363772-01	LED Assembly, Power On, Desk Top	
363772-02	LED Assembly, Power On, A4000	
391033-02	LED, Green	
903756-02	Wire, AWG #24, Red, 550mm	L=550.0
903756-10	Wire, AWG #24, Black, 550mm	L=550.0
903351-01	Connector Housing, 3 Pin	
903353-01	Pin	
363784-01	Crimper, LED	
903756-09	Wire, AWG #24, White, 400mm	L=400.0
903756-10	Wire, AWG #24, Black, 400mm	L=400.0

LED Assembly, Hard Disk Drive (363773 Rev 3)

363773-01	LED Assembly, Hard Disk Drive, Desk Top	
363773-02	LED Assembly, Hard Disk Drive, A4000	
391033-01	LED, Yellow	
903756-02	Wire, AWG #24, Red 550mm	L=550.0
903756-10	Wire, AWG #24, Black 550mm	L=550.0
903351-01	Connector Housing, 3 Pin	
903353-01	Pin	
363784-01	Crimper, LED	
903756-02	Wire, AWG #24 Red 400mm	L=400.0
903756-10	Wire, AWG #24, Black, 400mm	L=400.0

Keyswitch Assembly (363774 Rev C)

363774-01	Keyswitch Assembly, Desk Top	
363774-02	Keyswitch Assembly, A4000	
364285-01	Switch, Keylock	W/2 Keys (Chrome)
903756-01	Wire, Lead AWG #24	L=250mm (Black)
903756-02	Wire, Lead AWG #24	L=250mm (Red)
903353-01	Pin, Connector	
903351-01	Housing, Connector, 3 Pin	
903756-01	Wire, Lead AWG #24	L=400mm (Black)
903756-06	Wire, Lead AWG #24	L=400mm (Blue)

Cable Assembly, Hard Disk Drive (364527 Rev B)

364527-01	Cable Assembly, H.D.D.	
364527-02	Cable Assembly, H.D.D., A4000	
903468-06	Connector, Dual Row, 40 Pin	
903135-13	Cable, Flat, 40 Position	L=160mm
903135-13	Cable, Flat, 40 Position	L=480mm

PCB Assembly, A4000 Daughter Board (364822 Rev B)

364822-01	PCB Assembly, A3400 Daughter Card	
364821-01	Schematic, A4000 Daughter Board	
364823-01	Artwork, A4000 Daughter Board	
364820-01	Fab, A4000 Daughter Board	
380227-01	IC, 74HCT32	U600
901522-30	IC, 7407	U601
380388-04	Resistor Network, SIP, 220/330, 8 x 10	RP602-RP607
380388-01	Resistor Network, SIP, 220/330, 4 x 6	RP608
380388-04	Resistor Network, SIP, 220/330, 8 x 10	RP608
902410-10	Resistor Network, SIP, 1K, 9 x 10	RP752 - RP756
902410-08	Resistor Network, SIP, 4.7K, 9 x 10	RP751
901550-58	Resistor, 1/4W, 470 Ohm	R601 R603
901550-01	Resistor, 1/4W, 1K Ohm	R600 R602 R605 R606 R607 R608 R610
900462-61	Capacitor, Ceramic Axial 1000 pF axial	C756 - C799
390082-01	Capacitor, Ceramic Axial .1 uF axial	C604 C606
900101-53	Capacitor, Electrolytic Axial 22uF 16V	C751 C752
900101-47	Capacitor, Electrolytic Axial 220uF 16V	C600-C602
903446-04	Connector, Card Edge 36 Pin	CN621 CN754 CN755 CN756
903446-08	Connector, Card Edge 54 Pin	CN622
903446-02	Connector, Card Edge 62 Pin	CN751 - CN753
903446-06	Connector, Card Edge 100 Pin	CN600-CN603
903025-01	Ferrite Bead, Axial	FB601

Base (Basic) Assembly, A4000 (364828 Rev B)

364828-01	Base (Basic) Assembly, A4000
363851-01	Chassis
364073-01	Bezel, Front
363850-01	Cover

Base (Basic) Assembly, A4000 (364828 Rev B) (cont'd)

364859-01	Bracket, Option Card	
380120-01	Panel, Extension Card	
363818-02	Brace, Chassis Top	
364454-02	Bracket, Side Port	
364206-01	Bracket, FDD Support	
364465-01	Cover Plate, Rear Option	
363819-01	Support, HDD, Left Hand	
363819-02	Support, HDD, Right Hand	
380742-05	Cable, Assembly, FDD	
364822-01	Card, Expansion Slot Riser	
363830-01	Button, Power	
364938-01	Insulation Sheet, HDD	Place between PN 363819-01& 364822-01
364231-01	Insulation Sheet	
251118-01	Guide, Card	
310080-01	Feet, Rubber	
363774-02	Keyswitch Assembly	Wrap 3 turns around PN 906115-08
369179-01	Label, Back Panel	
363772-02	LED Assembly, Power On	Wrap 3 turns around PN 906115-08
363773-02	LED Assembly, Hard Disk Drive	Wrap 3 turns around PN 906115-08
906800-05	Screw, 3Mx6.0 MACH.PHL PAN HD	Fasten PN 363850-01 to 363851-01
906800-01	Screw, 3Mx4.0 MACH.PHL PAN HD	For PN 364859-01
390329-01	Screw, 3.5Mx5.0 PHL PAN HD	For PN 380120-01 to PN 364859-01
906800-07	Screw, M3 x 5.0	Fasten PN 363818-02, 364206-01, & 364465-01 to 363851-01
906803-01	Screw, 3Mx6.0 Flat Head	For PN 363819-01 & 363819-02 to 363818-02
906115-08	Toroid	
364509-01	Clip, Grounding	
390251-04	Standoff, HEX, M/F, M3x0.5/4-40	

PCB Assembly, 68020/68030 CPU Card (364832 Rev C)

364832-01	Processor Card, 25 MHz 68020, no FPU	
364832-02	Processor Card, 25 MHz 68020, 25 MHz 68882	
364832-03	Processor Card, 25 MHz 68030, no FPU	
364832-04	Processor Card, 25 MHz 68030, 25 MHz 68882	
364832-05	Processor Card, 25 Mhz, 68030, 68020, FPU, ROM ReMap	
364835-01	Schematic	
364834-01	PCB Fab	
364833-01	Artwork	
390818-06	Capacitor, SM, MLC, NPO, 100pF (1206)	C102
390818-02	Capacitor, SM, MLC, NPO, 220pF (1206)	C101B C104B C200C C202C
390853-01	Capacitor, SM. MLC, X7R, .01uF (1206)	C103A
310027-02	Capacitor, SM, Ceramic, 0.1uF (1206)	C100A C102A
390797-02	Capacitor, SM, Ceramic, Z5U, .22uF (1210)	C101A C104A C200A C202A
391097-03	Capacitor, SM, Elec. Alum. 22uF 16V 'C'	C101C C104C C200B C202B
310026-45	Resistor, Chip, 1/8W, 5%, 1 OHM (1206)	R103-R105 R202 R203

PCB Assembly, 68020/68030 CPU Card (364832 Rev C) (cont'd)		
310026-45	Resistor, Chip, 1/8W, 5%, 1 OHM (1206)	R103-R105 R204 R205
311026-01	Resistor, Chip, 1/8W, 5%, 47 OHM (1206)	R109 R112 R113
310026-05	Resistor, Chip, 1/8W, 5%, 100 OHM (1206)	R101 R102
310026-08	Resistor, Chip, 1/8W, 5%, 4.7K OHM (1206)	R100 R106 R107 R108 R110 R111
391321-04	Socket, SM PLCC for 68881/68882	U101; (Use Item 40 for AUTO-PLACE Assembly)
391413-03	IC, 68020 CPU, 132 QFP, 25MHz	U200
390399-04	IC, 68030 CPU, 132 QFP, 25 MHz	U202
390434-01	IC, MC68882 FPU 25 MHz PLCC	U101
391485-01	IC, PAL, 22V10-10 Programmed PLCC, ROM Remap	U100; Programmed into PN 391392-03
390868-01	IC, SMD, 74F174, SOIC	U102
391323-01	IC, SMD, 74F38, SOIC	U105
391321-08	Socket, SM, PLCC, W/O Mounting Posts	Sub for PN 391321-04 (for AUTO-PLACE Assembly)
	Not Stuffed	U103
903326-03	3 x .1" SIL	J103 J201-J203
903326-03	3 x .1" SIL	J100 J101
390556-01	Connector, 200 Pin KEL	CN10
390043-01	Shorting Bars (Shunts)	J100 J101
390043-01	Shorting Bars (Shunts)	J103 J201-J203

PCB Assembly, A4000 (364837 Rev E)		
364837-01	PCB Assembly, A4000 NTSC	
364837-02	PCB Assembly, A4000 PAL	
364836-01	Schematic	
364838-01	PCB Fab	
364839-01	Artwork	
	CAPACITORS	
390818-01	Capacitor, SM, MLC, NPO, 22pF (1206)	C485 C179
390818-04	Capacitor, SM, MLC, NPO, 47pF (1206)	EC976-EC989 EC350-EC364
390818-05	Capacitor, SM, MLC, NPO, 56pF (1206)	C178
390818-06	Capacitor, SM, MLC, NPO, 100pF (1206)	EC182-EC184 EC300-EC309 EC365-EC379 EC410 EC411 EC451-EC464
390818-10	Capacitor, SM, MLC, NPO, 330pF (1206)	C446, C447
390853-08	Capacitor, SM, MLC, X7R, 3900pF (1206)	C432 C442
390853-09	Capacitor, SM, MLC, X7R, 6800pF (1206)	C431 C441
390853-01	Capacitor, SM, MLC, X7R, .01uF (1206)	C104 C154B C186 C193 C195 C409 C460D C460E C460F
390853-04	Capacitor, SM, MLC, X7R, .047uF (1206)	C411-C414 C430 C440
310027-02	Capacitor, SM, Ceramic, 0.1uF (1206)	C102 C103 C106 C130 C131 C140 C141 C145 C152 C154A C177 C201 C205 C211A C211B C211C C212 C213 C215 C216 C250A C250C C300 C305 C311 C350-C355 C400B C402A C402B C455-C459 C460A C460B C460C C500 C860 C890-C894 C901-C904 C907 C975 C976 C990 C511-C513 C455B C456B C457B C458B

PCB Assembly, A4000 (364837 Rev E) (cont'd)

390797-02	Capacitor, SM, Ceramic, Z5U, .22uF (1210)	C150 C175 C176 C199 C403 C405 C406 C450 C700-C704 C706-C708 C710 C711 C714
391097-06	Capacitor, SM, Elec. Alum. 4.7uF 25V 'A'	C200 C404
391097-07	Capacitor, SM, Elec. Alum. 10uF 25V 'C'	C460G
391097-03	Capacitor, SM, Elec. Alum. 22uF 16V 'C'	C198 C317 C318 C433 C443
391097-04	Capacitor, SM, Elec. Alum. 47uF 16V 'D'	C187-C192 C194 C196 C407 C408
391097-01	Capacitor, SM, Elec. Alum. 100uF 6.3V 'D'	C181
390101-03	Capacitor, Elec. Alum. Radial 470uF 16V	C185 C400A
251029-06	Capacitor, Trimmer, Ceramic, 6.8-45pF	VC190
	TRANSISTORS, DIODES, FERRITES	
391121-01	IC, SMD, NPN, Transistor, 2N3904 (SOT23)	Q300 Q901
391122-01	IC, SMD, PNP, Transistor, 2N3906 (SOT23)	Q400
391145-01	Transistor, SM, N-Channel JFET MMBF102L	Q430 Q440
391327-01	Diode, SM, 1N4001 (MELF)	D175 D176 D305-D307 D360-D363, D500-D505
391129-01	Diode, SMT, 1N4148 (SOT23)	D177 D178 D300
391559-01	Filter, Ferrite, SMT (1812)	FB177 FB308 FB309 FB364-FB366 FB401 FB462 FB463 FB464 FB476 FB478-FB480 FB975
391092-03	Filter, Ferrite, SMT (1206)	FB710 FB410 FB411 ER976-ER989
391138-05	Inductor, SM, 47uH (1210)	L500
	RESISTORS	
391093-01	Resistor, SM, 1W, 5%, 1 Ohm (2512)	R400
391093-07	Resistor, SM, 1W, 5%, 20 Ohm (2512)	R176 R177
391093-04	Resistor, SM, 1W, 5%, 47 Ohm (2512)	R383
310026-45	Resistor, Chip, 1/8W, 5%, 1 Ohm (1206)	R403 R404
310026-24	Resistor, Chip, 1/8W, 5%, 120 Ohm (1206)	R311
310026-43	Resistor, Chip, 1/8W, 5%, 33 Ohm (1206)	R104 R211 R231-R237 R240-R248 R881-R899
310026-01	Resistor, Chip, 1/8W, 5%, 47 Ohm (1206)	R101-R103 R105 R106 R111 R112 R161 R162 R212-R218 R222 R223 R451 R458-R464 R500-R508 R513 R520-R543 R701-R704 ER175 R458A R458B R660 R661 ER176 ER300-ER307 ER350-ER363 ER367-ER379 ER453 ER458-ER461 ER475 R165-R170
391509-04	Resistor, Chip, 1/10W, 5%, 47 Ohm (0805)	R455A, R455B R455C R455D R455E R455F R455G R455H R456A R456B R456C R456D R456E R456F R456G R455H R457A R457B R457C R457D R457E R457F R457G R457H
310026-29	Resistor Chip, 1/8W, 5%, 75 Ohm (1206)	R510-R512
310026-30	Resistor, Chip, 1/8W, 5%, 220 Ohm (1206)	R301 R307
310026-21	Resistor, Chip, 1/8W, 5%, 470 Ohm (1206)	R120-R122 R175 R178 R651
310026-56	Resistor, Chip, 1/8W, 5%, 680 Ohm (1206)	R65 R66
310026-57	Resistor, Chip, 1/8W, 5%, 750 Ohm (1206)	R430 R440

PCB Assembly, A4000 (364837 Rev E) (cont'd)

310026-07	Resistor, Chip, 1/8W, 5%, 1.0K Ohm (1206)	R67 R68 R70-R73 R125-R128 R171-R173 R181 R182 R239 R249 R302 R371 R381 R382 R401 R402 R433 R434 R443 R444 R545-R548 R612-R626 R630-R635 R639 R708-R712 R720-R722 R861 R862 R911 R912 R975
310026-54	Resistor, Chip, 1/8W, 5%, 1.2K Ohm (1206)	R79-R88 R179 R405
310026-51	Resistor, Chip, 1/8W, 5%, 2.4K Ohm (1206)	R403D R403H
310026-16	Resistor, Chip, 1/8W, 5%, 2.7K Ohm (1206)	R1-R64 R74-R78 R206 R207 R407 R652 R871 R904 R905
310026-46	Resistor, Chip, 1/8W, 5%, 3.3K Ohm (1206)	R151 R360 R361
310026-08	Resistor, Chip, 1/8W, 5%, 4.7K Ohm (1206)	R515 R403C R403G R981-R994
310026-17	Resistor, Chip, 1/8W, 5%, 10 K Ohm (1206)	R208 R305 R306 R406 R408 R431 R432 R441 R442 R457 R465 R514 R403A R403B R403E R403F R355-R359
310026-55	Resistor, Chip, 1/8W, 5%, 11 K Ohm (1206)	R902 R903
310026-31	Resistor, Chip, 1/8W, 5%, 100K Ohm (1206)	R180
310026-19	Resistor, Chip, 1/8W, 5%, 470K Ohm (1206)	R435 R445
391154-27	Resistor, Chip, 1/8W, 1%, 562 Ohm (1206)	R509
902412-14	Res. Netwk., SIP, 9 Pin, 8 Element, 1K Ohm	RP461-RP463
902410-10	Res. Netwk., SIP, 10 Pin, 9 Element, 1K Ohm	RP351
902442-35	Res. Netwk., SIP, 8 Pin, 7 Element, 10K Ohm	RP176
325566-27	Oscillator, 50 MHz, T.H. Can	U104
325566-14	Oscillator, 28.63636 MHz, T.H. can	U154 (NTSC)
252344-01	Oscillator, 28.37516 MHz, T.H.can	U154 (PAL)
900560-01	Crystal, 32.768 KHz, T.H.	Y176
	INTEGRATED CIRCUITS	
391513-02	IC, Kickstart ROM (LOW) 150ns	U176 Set J151 = Pins 2-3 (V39.106)
391514-02	IC, Kickstart ROM (HIGH) 150ns	U175 Set J151 = Pins 2-3 (V39.106)
391010-01	IC, CSG, 8374, ALICE, 84 Pin PLCC	U211
391227-01	IC, CSG, 4203, LISA, 84 Pin PLCC	U450
391077-01	IC, 8364R7 PAULA PLCC 52	U400
391078-02	IC, SM, LSI, Complex Int Adapt 8520A-1 PLCC 44	U300 U350
390525-01	IC, Ricoh, Real Time Clock, RP5C01, DIP	U178
391494-01	IC, Video DAC, Triple 8-BIT, ADV7120, PLCC 44	U460
390540-02	IC, LSI, FAT GARY, F008B, PLCC84	U150
390541-07	IC, FAT RAMSEY, F012G, PLCC 84	U890
391380-01	IC, BRIDGETTE, PQFP 100	U250
390539-09	IC, LSI, FAT BUSTER, FO13I, PLCC84	U700
391473-01	IC, SMD, Op Amp, Dual, LM833	U403
391103-01	IC, SMD, Op Amp, Quad JFET, LF347	U402
390555-01	Delay Line, 5 Tap, 25ns, DIP	U102
391087-01	IC, SMD, Quad Line Driver, 1488 SOIC	U304
391086-01	IC, SMD, Quad Line Receiver, 1489 SOIC	U305
391421-01	Voltage Reference, 1.2V, SO-8	D507

PCB Assembly, A4000 (364837 Rev E) (cont'd)

901527-03	IC, Voltage Regulator, Fixed Output, TO-220, 7905	U198
391554-01	IC, Linear, LF347, EIAJ Package	Sub for PN 391103-01
391478-01	IC, PAL, 22V10-10 Programmed PLCC,Chip CAS Gen	U212; Programmed into PN 391392-03
391477-01	IC, PAL, 16L8-10 Programmed PLCC, Chip RAM Ctrl	U213; Programmed into PN 391412-01
391476-01	IC, PAL, 16R4-15 Programmed PLCC, Arb & int.	U701; Programmed into PN 391359-04
391475-01	IC, PAL, 16L8-10 Programmed PLCC, Zorro Decode	U714; Programmed into PN 391199-03
391406-01	IC, PAL, 16L8-15 Programmed PLCC, IDE Decode	U901; Programmed into PN 391199-04
391405-01	IC, PAL, 16R6-15 Programmed PLCC, IDE state	U902; Programmed into PN 391403-02
391276-01	7406, SOIC package	U131
391188-01	7407, SOIC package	U311 U141
391499-01	74F521, SOIC package	U145
391088-01	74F04, SOIC package	U215
391183-01	74F08, SOIC package	U130 U710
391175-01	74F32, SOIC package	U140
391320-01	74F74, SOIC package	U106 U459
391325-01	74F86, SOIC package	U711
391375-01	74F245, SOIC package	U704 U707 U708 U891-U894
391481-01	74F841, SOIC package	U216
391374-02	74FCT646T, SOIC package	U702 U703 U706
391480-01	74HCT166, SOIC package	U975-U976
391400-01	74FCT244T, DIP package	U103
391474-01	74FCT245T, SOIC package	U455-U458
391377-01	74HCT174, SOIC package	U177 U354 U907
391326-01	74LS38, SOIC package	U352
391141-01	74LS74A, SOIC package	U351
391311-01	74HC4066, SOIC package	U205
391100-01	74HCT245, SOIC package	U903 U904
391191-01	74LS125A, SOIC package	U353 U355
391548-01	74F86, SM, EIAJ package	Substitute for PN 391325-01
391552-01	74HCT174, SM, EIAJ Package	Substitute for PN 391377-01
391555-01	74LS74A, SM, TTL, EIAJ Package	Substitute for PN 391141-01
	SOCKETS	
390768-04	Socket, 20 Pin .3 DIP machine pin	U103 (Clock distribution)
904150-06	Socket, 40 Pin .6 DIP	U175 U176 (ROMs)
391368-01	Socket, 72 Pin 22.5 Deg. SIMM	U261 U850-U853
390719-01	Socket, single pin (.040 hole)	U104 U154
	MISC ELECTRICAL	
380393-02	Battery, NICAD, Rechargeable, 3.6V	BT176
380393-03	Battery, NICAD, Rechargeable, 3.6V	BT176
390924-01	Varistor Switch, Self Resetting 1.85A	F175
	CONNECTORS	
903345-06	12 DIL .1" x .1" Header	J975
903345-17	34 DIL .1" x .1" Header	CN351

PCB Assembly, A4000 (364837 Rev E) (cont'd)

903345-20	40 DIL .1" x .1" Header	CN900
903326-02	2 x .1" SIL	J351 J850
903326-03	3 x .1" SIL	CN404 J100 J104 J151 J212-J214 J352 J500-J502 J852 CN200 CN302 CN303
390242-01	DB9 Male	CN975 CN976
390242-03	DB23 Male	CN450
390241-03	DB23 Female	CN352
390625-04	Stacked DB25 Male/Female (missionary)	CN350+CN300
390851-04	6 Pin MINI DIN, Female	CN175
390043-01	Shorting Bars (Shunts)	J100 J104 J120 J151 J152 J212 J214 J352 J850 J852
903349-01	6 Pin Connector (Power In)	CN160
252122-02	RCA Jack (Red)	CN403
252122-01	RCA Jack (White)	CN402
903446-06	100 Pin Edge Card Connector	CN452 CN600
390557-01	200 Pin KEL Connector	CN651
	UNSTUFFED COMPONENTS	
	R465	
	C406H	

PCB Assembly, 68040 CPU Card (364856)

364856-01	PCB Assembly, 68040 CPU Card, 68040	
364856-02	PCB Assembly, 68040 CPU Card, 68EC040	
364853-01	Schematic	
364855-01	PCB Fab	
364854-01	Artwork	
	CAPACITORS	
390853-01	Capacitor, SM, MLC, X7R, .01uF (1206)	C100A
390818-06	Capacitor, SM, MLC, NPO, 100pF (1206)	C400
310027-02	Capacitor, SM, Ceramic, 0.1uF (1206)	C101A C103A C104A C105A C200A C201A C202A C203A C204 C205 C206A C207 C208A C209 C211 C213 C400A C401A C402A
390797-01	Capacitor, SM, Ceramic, Z5U, .33uF (1210)	C212A C214A C215A C216A C217A C218A C219A C220A C221A C222A C101B
390797-02	Capacitor, SM, Ceramic, Z5U, .22uF (1210)	C102D C102A
390818-02	Capacitor, SM, MLC, NPO, 220pF (1206)	C102C C102F
391097-03	Capacitor, SM, Elec. Alum., 22uF 16V 'C'	C105 C106 C107 C102E C102B
	RESISTORS	
310026-43	Resistor, Chip, 1/8W, 5%, 33 Ohm (1206)	R107, R108
310026-05	Resistor, Chip, 1/8W, 5%, 100 Ohm (1206)	R400 R401
310026-21	Resistor, Chip, 1/8W, 5%, 470 Ohm (1206)	R402 R403 R404
310026-08	Resistor, Chip, 1/8W, 5%, 4.7K Ohm (1206)	R104 R105 R106 R405
310026-06	Resistor, Chip, 1/8W, 5%, 22 Ohm (1206)	R101 R102
310026-45	Resistor, Chip, 1/8W, 5%, 1 Ohm (1206)	R100 R103
902410-10	Res. Ntwk,SIP, 10 Pin, 9 Element, 1K Ohm	RP100 RP400 RP401 RP402 RP403 RP404 RP405

PCB Assembly, 68040 CPU Card (364856) (cont'd)

326149-01	Res. Ntwk, SIP, 8 Pin, 4 Element, 22 Ohm	RP102 RP103 RP104 RP105 RP101 RP106 RP107 RP108
	INTEGRATED CIRCUITS TTL	
390789-02	IC, SMD, 74FCT244AT	U402
390784-02	IC, SMD, 74FCT374AT	U201
390786-02	IC, SMD, 74FCT373AT	U200
391175-01	IC, SMD, 74F32	U202
391495-01	IC, SMD, 74F257	U212
391176-01	IC, SMD, 74F139	U206
391088-01	IC, SMD, 74F04	U105
391188-01	IC, SMD, 7407	U104
391487-01	IC, SMD, 74FCT543T	U214 U215 U216 U217 U218 U219 U220 U221 U222
391486-01	IC, SMD, 74F1803	U101
	ICs MISC	
390555-01	Delay Line 5 Tap 25ns, DIP	U103
325566-27	Oscillator, Crystal controlled, 50MHz	U100
	HEADERS	
903326-03	3 x .1" SIL	J400
903326-04	4 x .1" SIL	J100
903326-02	2 x .1" SIL	TJ100
	OTHER CONNECTORS	
390043-01	Shorting Bars	J100 J400 TJ100
390556-01	200 Pin KEL Connector (Male)	CONN200
	FERRITES	
391092-01	Filter,Ferrite,SMT (1812)	FB100 FB200
	SOCKETS	
391492-01	Socket 179 Pin PGA for 68040	Sub for PN 390296-09
391493-01	Heat Sink and Clip for 68040 Socket	Sub for PN 391493-02 use w/ PN 391492-01
390296-09	Socket 179 Pin PGA	U102
391493-02	Heat Sink and Clip	U102 Use w/ PN 390296-09 or 391492-01
	MICROPROCESSORS	
390796-01	MC68040	U102
391466-01	MC68EC040	U102
	PALs	
391467-01	IC, PAL, 22V10-15 Programmed PLCC, TAXLAT	U213
391468-01	IC, PAL, 22V10-15 Programmed PLCC, OEBUS	U207
391469-01	IC, PAL, 22V10-15 Programmed PLCC, MAPPER	U400
391470-01	IC, PAL, 22V10-10 Programmed PLCC, BUSCON	U204
391471-01	IC, PAL, 22V10-10 Programmed PLCC, BUSTERM	U205
391472-01	IC, PAL, 22V10-10 Programmed PLCC, BCTL	U209
391491-01	IC, PAL, 22V10-10 Programmed PLCC, START	U211
391490-01	IC, PAL, 16V8-10 Programmed PLCC, TERM	U203
391489-01	IC, PAL, 16V8-10 Programmed PLCC, LEBUS	U208
391488-01	IC, PAL, 16V8-10 Programmed PLCC, RST	U401

PCB Assembly, 68040 CPU Card (364856) (cont'd)

	J100 (*CDIS *MDIS)	Short pins 1-2 & pins 3-4
	J400 (MAPROM) 1-2 Enabled, 2-3 Disabled	Short pins 1-2
	TJ100 (TEST)	Short pins 1-2

Software Assembly, Level 3 Amiga V3.0 (364870 Rev B)

364870-01	Software Assembly, Level 3	US
364870-02	Software Assembly, Level 3	Canada Inactive
364870-03	Software Assembly, Level 3	UK Inactive
364870-04	Software Assembly, Level 3	German
364870-05	Software Assembly, Level 3	French
364870-06	Software Assembly, Level 3	Italian
365039-01	Slipcase	
365038-01	Disk Sub Assembly, Level 3, Amiga V3.0	
368763-01	Manual, AmigaDOS	English
368766-01	Manual, AmigaDOS	German
368764-01	Manual, AmigaDOS	French
368765-01	Manual, AmigaDOS	Italian
368759-01	Manual, Amiga ARexx	English
368762-01	Manual, Amiga ARexx	German
368760-01	Manual, Amiga ARexx	French
368761-01	Manual, Amiga ARexx	Italian
368914-01	Manual, Workbench V3.0	English
368917-01	Manual, Workbench V3.0	German
368915-01	Manual, Workbench V3.0	French
368916-01	Manual, Workbench V3.0	Iitalian
366947-01	Label, Part Number	English
366949-01	Label, Part Number	German
366948-01	Label, Part Number	French
366950-01	Label, Part Number	Italian
318757-17	Shrink Wrap	*A/R
368759-01	Manual, ARexx 2.04	English
368760-01	Manual, ARexx 2.04	French
368761-01	Manual, ARexx 2.04	Italian
368762-01	Manual, ARexx 2.04	German

Drive Cable Assembly II (380742 Rev K)

380742-01	Drive Cable Assembly II, Amiga 2000 for Matsushita JU363-282/Chinon F354	
380742-02	Drive Cable Assembly II, Amiga 2000 for Matsushita JU253-02T/Chinon FB354	
380742-03	Drive Cable Assembly, Amiga 3000	
380742-04	Drive Cable Assembly, Amiga 3500	
380742-05	Drive Cable Assembly, Amiga 4000	
903135-10	Flat Cable, 34 POL.	L=570mm
903468-05	Dual Row Connector, 34 Pin	Amp No. 3-164703-4 or Equiv.
380328-01	Keying Plug	Amp No. 926329-1 or Equiv.

Drive Cable Assembly II (380742 Rev K)		(cont'd)
903135-10	Flat Cable, 34 Conductors	L=450mm
903135-10	Flat Cable, 34 Conductors	L=475mm
903135-10	Flat Cable, 34 Conductors	L=715mm

A4000/020 (534802 Rev B)		
534802-01	A4000/020 U.S. Without HDD, 1M + 1M	
534802-02	A4000/020 U.S. With HDD 50MB, 1M + 1M	
534802-03	A4000/020 EU. Without HDD, 1M + 1M	
534802-04	A4000/020 EU. With HDD 50MB, 1M + 1M	
364828-01	Base Assembly	
313248-03	Floppy Disk Drive 3.5" 1.7 MB, 32mm	
365019-01	Floppy Disk Drive 3.5" 1.7 MB, 25mm	
364904-01	Bezel Cover, 5.25" Floppy Disk	
364239-01	Bezel Cover, 3.5" Floppy Disk 25mm	Use with PN 365019-01
364527-01	Bezel Cover, 3.5" Floppy Disk 32mm	Use with PN 313248-03
364527-01	Cable Assembly, Hard Disk Drive	
364837-01	PCB Assembly, NTSC	
364837-02	PCB Assembly, PAL	
391173-01	Power Supply, NTSC	
391173-02	Power Supply, PAL	
365018-01	Nameplate, A4000	
364339-03	Packing Box, A4000	
364201-01	Endcap	
364832-01	PCB Assembly, 68020 CPU Card	
369274-01	Label, Rating-Made In Germany	120V Product
369274-02	Label, Rating-Made In Hong Kong	120V Product
369274-03	Label, Rating-Made In Phillipines	120V Product
369274-04	Label, Rating-Made In Germany	240V Product
369274-05	Label, Rating-Made In Hong Kong	240V Product
369274-06	Label, Rating-Made In Phillipines	240V Product
369274-08	Label, Rating-Made In UK	240V Product
251006-01	Bag, Plastic	For Keyswitch Keys
325090-02	Seal, Warranty	
368084-01	Seal,Tamper Evident	Place on Box Flaps
906883-02	Screw, M3 x 4.0, Self Tapping	For Bezel Covers
906610-04	Screw, #6-32 x .25LG	For HDD
906800-05	Screw, M3x.05 x 6.0LG	For FDD
364861-01	Standoff, Plastic	For CPU Card
320408-04	Bag, Flat 650mm x 650mm	For CPU
324257-01	Bag, Drying Agent	Place into PN 320408-04
368803-01	Label, Gold Service	US Only
391396-01	IC, SIMM Module, 256K x 32, 80ns	U261, U853 (set J852 to 2-3)
390682-01	Video Adapter, 15 Pin to 23 Pin	Place in PN 320408-04
311839-01	Hard Disk Drive, 3.5", 52MB, 1", Quantum LPS52AT	
316583-07	Label, Hard Disk Drive	Quantum Prodrive 52AT
369478-02	Label, UPC, No Hard Disk Drive	Without FPU
369478-01	Label, UPC, 50MB	Without FPU

A4000/030 (534803 Rev C)

534803-01	A4000/030 U.S. Without HDD, 1M + 1M, No FPU	
534803-02	A4000/030 U.S. With HDD 50MB, 1M + 1M, No FPU - Inactive	
534803-03	A4000/030 EU. Without HDD, 1M + 1M, No FPU	
534803-04	A4000/030 EU. With HDD 50MB, 1M + 1M, No FPU - Inactive	
534803-05	A4000/030 U.S. With HDD 40MB, 2M + 2M, No FPU	
534803-06	A4000/030 EU. With HDD 40MB, 2M + 2M, No FPU	
534803-07	A4000/030 U.S. With HDD 80MB, 2M + 2M, No FPU	
534803-08	A4000/030 EU. With HDD 80MB, 2M + 2M, No FPU	
534803-09	A4000/030 U.S. With HDD 120MB, 2M + 2M, No FPU	
534803-10	A4000/030 EU. With HDD 120MB, 2M + 2M, No FPU	
534803-11	A4000/030 U.S. With HDD 200MB, 2M + 2M, No FPU	
534803-12	A4000/030 EU. With HDD 200MB, 2M + 2M, No FPU	
534803-13	A4000/030 U.S. With HDD 40MB, 2M + 2M, FPU	
534803-14	A4000/030 EU. With HDD 40MB, 2M + 2M, FPU	
534803-15	A4000/030 U.S. With HDD 80MB, 2M + 2M, FPU	
534803-16	A4000/030 EU. With HDD 80MB, 2M + 2M, FPU	
534803-17	A4000/030 U.S. With HDD 120MB, 2M + 2M, FPU	
534803-18	A4000/030 EU. With HDD 120MB, 2M + 2M, FPU	
534803-19	A4000/030 U.S. With HDD 200MB, 2M + 2M, FPU	
534803-20	A4000/030 EU. With HDD 200MB, 2M + 2M, FPU	
534803-21	A4000/030 U.S. With HDD 100MB, 2M + 2M, No FPU	
534803-22	A4000/030 EU. With HDD 100MB, 2M + 2M, No FPU	
534803-23	A4000/030 U.S. With HDD 100MB, 2M + 2M, FPU	
534803-24	A4000/030 EU. With HDD 100MB, 2M + 2M, FPU	
364828-01	Base Assembly	
365019-01	Floppy Disk Drive 3.5" , 1.7 MB, 25mm	
313248-03	Floppy Disk Drive 3.5" , 1.7 MB, 32mm	Sub for PN 365019-01
364904-01	Bezel Cover, 5.25" Floppy Disk	
364239-01	Bezel Cover, 3.5" Floppy Disk, 25mm	Use with PN 365019-01
364905-01	Bezel Cover, 3.5" Floppy Disk, 32mm	Use with PN 313248-03
364527-02	Cable Assembly, Hard Disk Drive	
364837-01	PCB Assembly, NTSC	Set J100 & J104 to pins 1-2
364837-02	PCB Assembly, PAL	
391173-01	Power Supply, NTSC	
391173-02	Power Supply, PAL	

A4000/030 (534803 Rev C) **(cont'd)**

365018-02	Nameplate, A4000/030	
364339-03	Packing Box, A4000	
364201-01	Endcap	
364832-03	PCB Assembly, 68030 CPU Card, No FPU	
364832-04	PCB Assembly, 68030 CPU Card, With FPU	
369274-01	Label, Rating-Made In Germany	120V Product
369274-02	Label, Rating-Made In Hong Kong	120V Product
369274-03	Label, Rating-Made In Phillipines	120V Product
369274-07	Label, Rating-Made In UK	120V Product
369274-04	Label, Rating-Made In Germany	240V Product
369274-05	Label, Rating-Made In Hong Kong	240V Product
369274-06	Label, Rating-Made In Phillipines	240V Product
369274-08	Label, Rating-Made In UK	240V Product
369619-01	Label, Ni-Cd	Place next to PN 369274-01 to 369274-06
251006-01	Bag, Plastic	For Keys of Keyswitch
325090-02	Seal, Warranty	
368084-01	Seal,Tamper Evident	Place on Box Flaps
906883-02	Screw M3 x 4.0, Self Tapping	For Bezel Covers
906610-04	Screw, #6-32 x .25LG	For HDD
906800-05	Screw, M3x.05 x 6.0LG	For FDD
364861-01	Standoff, Plastic	For CPU Card
320408-04	Bag,Flat 650mm x 650mm	For CPU
324257-01	Bag,Drying Agent	Place into PN 320408-04
368803-01	Label, Gold Service	US Only
391396-01	IC, SIMM Module, 256K x 32 80ns	U261 U853, SET J852 TO 2-3
391396-01	IC, SIMM Module, 256K x 32 80ns	U853 U852, SET J852 TO 2-3
391517-01	IC, SIMM Module, 512K x 32 80ns	U261
390682-01	Video Adapter 15 Pin to 23 Pin	Place in PN 320408-04
364290-01	3.5" Hard Disk, 1", 40MB, Seagate ST351A	
316583-09	Label, HDD "40 MB, Seagate ST351A"	Use with PN 364290-01
312966-03	3.5" Hard Disk, 1", 80MB, Seagate ST3096A	
312966-02	3.5" Hard Disk, 1", 80MB, WD WDAC280	Sub for PN 312966-03
316583-12	Label, HDD "80 MB Seagate ST3096A"	Use with PN 312966-03
316583-13	Label, HDD "80MB WD WDAC280"	Sub for PN 316583-12
364517-03	3.5" Hard Disk, 1", 120MB, Seagate ST3144A	
316583-15	Label, HDD "120 MB Seagate ST3144A"	Use with PN 364517-03
311639-04	3.5" Hard Disk, 1.625", 200MB, WD WDAC2200	
316583-20	Label, HDD WD WDAC2200	
369478-02	Label, UPC, Without HDD, No FPU	
369478-01	Label, UPC, 50MB HDD, No FPU	
369478-03	Label, UPC, 40MB HDD, No FPU	
369478-04	Label, UPC, 80MB HDD, No FPU	
369478-05	Label, UPC, 120MB HDD, No FPU	
369478-06	Label, UPC, 200MB HDD, No FPU	
369478-07	Label, UPC, 40MB HDD, With FPU	
369478-08	Label, UPC, 80MB HDD, With FPU	
369478-09	Label, UPC, 120MB HDD, With FPU	

A4000/030 (534803 Rev C) (cont'd)

369478-10	Label, UPC, 200MB HDD, With FPU	
369478-11	Label, UPC, 100MB HDD, No FPU	
369478-12	Label, UPC, 100MB HDD, With FPU	
311840-02	3.5" HDD, 100MB, Seagate ST3120A	
316583-21	Label, HDD, 100MB, Seagate ST3120A	

A4000/040 (534804 Rev C)

534804-01	A4000/040 U.S. Without HDD, 1M + 1M	
534804-02	A4000/040 U.S. With HDD 50MB, 1M + 1M - Inactive	
534804-03	A4000/040 EU. Without HDD, 1M + 1M	
534804-04	A4000/040 EU. With HDD 50MB, 1M + 1M - Inactive	
534804-05	A4000/040 U.S. With HDD 40MB, 2M + 4M	
534804-06	A4000/040 EU. With HDD 40MB, 2M + 4M	
534804-07	A4000/040 U.S. With HDD 80MB, 2M + 4M	
534804-08	A4000/040 EU. With HDD 80MB, 2M + 4M	
534804-09	A4000/040 U.S. With HDD 120MB, 2M + 4M	
534804-10	A4000/040 EU. With HDD 120MB, 2M + 4M	
534804-11	A4000/040 U.S. With HDD 200MB, 2M + 4M	
534804-12	A4000/040 EU. With HDD 200MB, 2M + 4M	
534804-13	A4000/040 U.S. With HDD 100MB, 2M + 4M	
534804-14	A4000/040 EU. With HDD 100MB, 2M + 4M	
364828-01	Base Assembly	
365019-01	Floppy Disk Drive 3.5", 1.7 MB, 25mm	
313248-03	Floppy Disk Drive 3.5", 1.7 MB, 32mm	Sub for PN 365019-01
364904-01	Bezel Cover, 5.25" Floppy Disk	
364239-01	Bezel Cover, 3.5" Floppy Disk, 25mm	Use with PN 365019-01
364905-01	Bezel Cover, 3.5" Floppy Disk, 32mm	Use with PN 313248-03
364527-02	Cable Assembly, Hard Disk Drive	
364837-01	PCB Assembly, NTSC	Set J100 & J104 Pins 2-3
364837-02	PCB Assembly, PAL	Remove U104 for 040 Card
391173-01	Power Supply, NTSC	
391173-02	Power Supply, PAL	
365018-03	Nameplate, A4000/040	
364339-03	Packing Box, A4000	
364201-01	Endcap	
364856-01	PCB Assembly, 68040 CPU Card	
369274-01	Label, Rating-Made In Germany	120V Product
369274-02	Label, Rating-Made In Hong Kong	120V Product
369274-03	Label, Rating-Made In Phillipines	120V Product
369274-07	Label, Rating-Made In UK	120V Product
369274-04	Label, Rating-Made In Germany	240V Product
369274-05	Label, Rating-Made In Hong Kong	240V Product
369274-06	Label, Rating-Made In Phillipines	240V Product
369274-08	Label, Rating-Made In UK	240V Product
369619-01	Label, Ni-Cd	Place next to PN 369274-01 to 369274-08

A4000/040 (534804 Rev C) (cont'd)

251006-01	Bag, Plastic	For keys of keyswitch
325090-02	Seal, Warranty	
368084-01	Seal,Tamper Evident	Place on box flaps
906883-02	Screw M3 x 4.0, Self Tapping	For Bezel Covers
906610-04	Screw, #6-32 x .25LG	For HDD
906800-05	Screw, M3 x .05 x 6.0LG	For FDD
364861-01	Standoff, Plastic	For CPU Card
320408-04	Bag, Flat 650mm x 650mm	For CPU
324257-01	Bag, Drying Agent	Place into PN 320408-04
368803-01	Label, Gold Service	US Only
391518-01	IC, SIMM Module, 1M x 32 80ns	U853 , Set J852 TO 1-2
391517-01	IC, SIMM Module, 512K x 32 80ns	U261
390682-01	Video Adapter 15 Pin to 23 Pin	Place in PN 320408-04
364290-01	3.5" Hard Disk, 1", 40MB, Seagate ST351A	
316583-09	Label, HDD "40 MB, Seagate ST351A"	Use with PN 364290-01
312966-03	3.5" Hard Disk, 1", 80MB, Seagate ST3096A	
312966-02	3.5" Hard Disk, 1", 80MB, WD WDAC280	Sub for PN 312966-03
316583-12	Label,HDD "80 MB Seagate ST3096A"	Use with PN 321966-03
316583-13	Label,HDD "80MB WD WDAC280"	Use with PN 312966-02
364517-03	3.5" Hard Disk, 1", 120MB, Seagate ST3144A	
316583-15	Label,HDD "120 MB Seagate ST3144A"	Use with PN 364517-03
311639-04	3.5" Hard Disk, 1.625", 200MB,WD WDAC2200	
316583-20	Label, HDD, 200MB, WD WDAC2200	
369477-02	Label, UPC, Without HDD	
369477-01	Label, UPC, 50MB HDD	
369477-03	Label, UPC, 40MB HDD	
369477-04	Label, UPC, 80MB HDD	
369477-05	Label, UPC, 120MB HDD,	
369477-06	Label, UPC, 200MB HDD	
369477-07	Label, UPC, 100MB HDD	
316583-21	Label, HDD, 100MB, Seagate ST3120A	
311840-02	3.5" HDD 100MB Seagate ST3120A	

Keyboard Ship Assembly, A4000 (582027 Rev D)

582027-01	Keyboard Ship Assembly	US
582027-02	Keyboard Ship Assembly	Canada
582027-03	Keyboard Ship Assembly	UK
582027-04	Keyboard Ship Assembly	German
582027-05	Keyboard Ship Assembly	French
582027-06	Keyboard Ship Assembly	Italian
582027-07	Keyboard Ship Assembly	Spanish
582027-08	Keyboard Ship Assembly	Swiss German
582027-09	Keyboard Ship Assembly	Swiss French
582027-10	Keyboard Ship Assembly	Austrian
582027-11	Keyboard Ship Assembly	Norwegian
582027-12	Keyboard Ship Assembly	Swedish
582027-13	Keyboard Ship Assembly	Finnish

Keyboard Ship Assembly, A4000 (582027 Rev D) (cont'd)

582027-14	Keyboard Ship Assembly	Dutch
582027-15	Keyboard Ship Assembly	Danish
582027-16	Keyboard Ship Assembly	Belgium French
582027-17	Keyboard Ship Assembly	Belgium Dutch
582027-18	Keyboard Ship Assembly	Australian
582027-19	Keyboard Ship Assembly	CEL
582027-20	Keyboard Ship Assembly	Portuguese
364447-01	Keyboard Assembly	US
364447-02	Keyboard Assembly	UK
364447-03	Keyboard Assembly	German
364447-05	Keyboard Assembly	French
364447-04	Keyboard Assembly	Italian
364447-06	Keyboard Assembly	Spanish
364447-07	Keyboard Assembly	Swedish
364447-09	Keyboard Assembly	Norwegian
364447-10	Keyboard Assembly	Swedish/Finnish
364447-08	Keyboard Assembly	Danish
366981-01	Label, Carton, US	US
366981-02	Label, Carton, Canada	Canada
366981-03	Label, Carton, UK	UK
366981-04	Label, Carton, Germany	German
366981-05	Label, Carton, France	French
366981-06	Label, Carton, Italy	Italian
366981-07	Label, Carton, Spain	Spanish
366981-08	Label, Carton, Swiss German	Swiss German
366981-09	Label, Carton, Swiss French	Swiss French
366981-10	Label, Carton, Austria	Austrian
366981-11	Label, Carton, Norway	Norwegian
366981-12	Label, Carton, Sweden	Swedish
366981-13	Label, Carton, Finland	Finnish
366981-14	Label, Carton, Netherlands	Dutch
366981-15	Label, Carton, Denmark	Danish
366981-16	Label, Carton, Belgium, French	Belgium French
366981-17	Label, Carton, Belgium Dutch	Belgium Dutch
366981-18	Label, Carton, Australia	Australian
366981-19	Label, Carton, CEL Trade	CE
366981-20	Label, Carton, Portugal	Portuguese
318243-01	Endcap, Keyboard	
380425-03	Container, Shipping	
251006-02	Bag, Flat, 580mm x 350mm	
324252-07	Tape, Adhesive Transparent, 50mm	
327124-05	Mouse Assembly, 1.2M Cable, Limestone Beige, No Ferrite	Sub for PN 327124-07 (-01 & -02)
327124-07	Mouse Assembly, 1.2M Cable, Limestone Beige, w/Ferrite	
327124-17	Mouse Assembly, 1.2M Cable, Limestone Beige, w/Ferrite	Sub for PN 327124-05 & 327124-07
364870-01	Amiga Software Assembly, Level 3 V3.0	English

Keyboard Ship Assembly, A4000 (582027 Rev D) (cont'd)

364870-04	Amiga Software Assembly, Level 3 V3.0	German
364870-05	Amiga Software Assembly, Level 3 V3.0	French
364870-06	Amiga Software Assembly, Level 3 V3.0	Italian
371115-01	FTZ Statement Sheet	German
400804-01	Service Sub-Assembly	US
318882-02	Warranty Card	Canada
325349-01	Warranty Card	UK
320046-06	Warranty Card	German
325254-01	Warranty Card	French
368014-02	Warranty Card	Australian
380933-01	Warranty Card	Swedish
318876-02	Service Center List	Australian
318896-04	Software License Agreement	
318708-01	Software License Agreement	German
318556-02	Disk Exchange Card	Canada
312341-02	Disk Exchange Card	US
903508-18	Power Cord, Black US/Canada	UL/CSA
903508-21	Power Cord, Black UK	BSI
903508-19	Power Cord, Black	VDE
903508-20	Power Cord, Black Switzerland	SEV
903508-22	Power Cord, Black Australia	
368924-01	Manual, User's Guide A4000	English
368927-01	Manual, User's Guide A4000	German
368925-01	Manual, User's Guide A4000	French
368926-01	Manual, User's Guide A4000	Italian
371023-01	Manual, User's Guide A4000	Swedish
371001-01	Manual, Hard Disk User's Guide	English
371004-01	Manual, Hard Disk User's Guide	German
371002-01	Manual, Hard Disk User's Guide	French
371003-01	Manual, Hard Disk User's Guide	Italian
371028-01	Manual, Hard Disk User's Guide	Swedish

Chapter 6

System Specification

A4000 Functional Specification

Description

The A4000 computer is a new member of the Amiga family, based on the AA chip set. It is housed in a desktop case with a separate keyboard. Expansion capabilities are provided via four internal Zorro II/III expansion connectors and a CPU slot.

A block diagram is shown in Figure 6-1.

Electrical Specifications

CPU

The CPU for the A4000 is contained on a separate CPU card. This allows a single motherboard to be combined with one of several CPU cards to create different system configurations. Currently, there are two different CPU cards available.

68020/68030 CPU Card

This card has PCB QFP footprints for both the MC68020 and the MC68030. Either (or both) of these two processors can be soldered to the board and used — a jumper on the CPU card selects between the 68020 or the 68030.

There are also two footprints for an optional 68881 or 68882 math coprocessor on this CPU card. The QFP PCB outline can be used for factory installed FPUs and the PGA footprint is available for user installations. A jumper on the CPU card selects between the two possible locations.

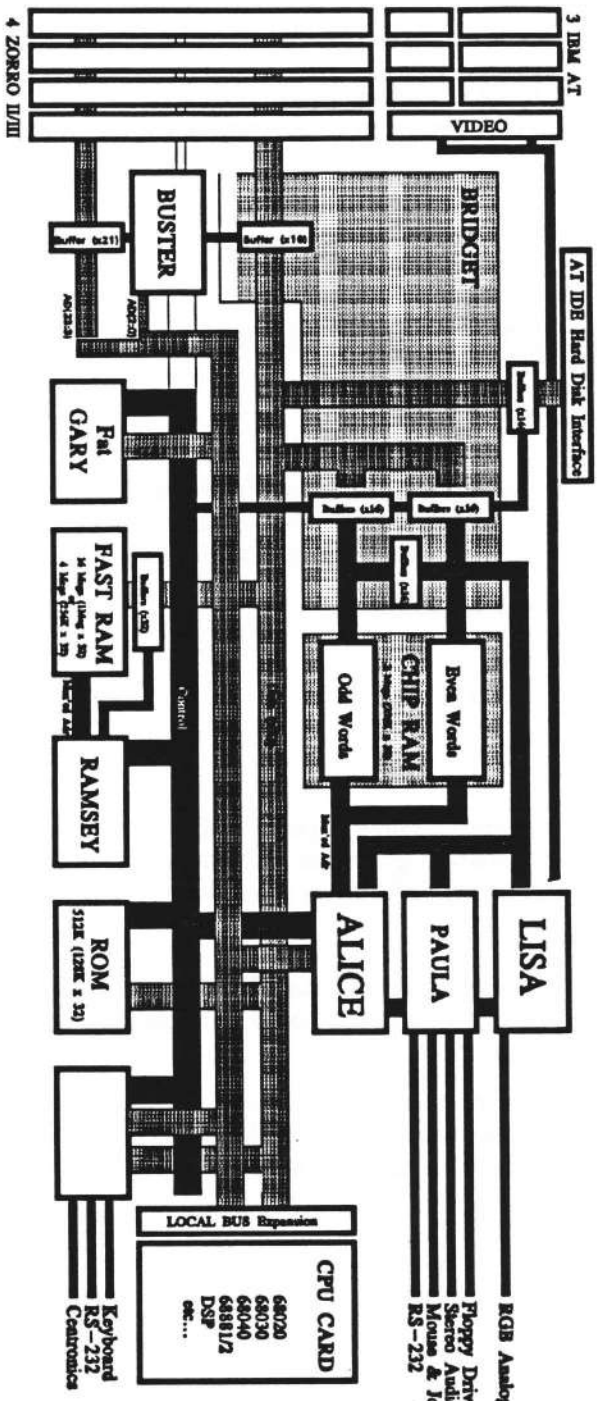


Figure 6-1. Amiga 4000 Block Diagram

Normally, the FPU is driven by the motherboard's 25 MHz clock. However, a separate oscillator can be installed by the user to clock the FPU at a higher rate. A jumper selects between the two different clock sources.

68040 CPU Card

This CPU card can be used with a 25 MHz 68040, 68EC040, 68LC040, or 68EC030. The '040 and '030 reside in a PGA socket.

Fast RAM

- Up to 16 Megabytes
- Four 72-pin SIMM sockets
- 32-bit CPU interface
- Page or Static Column mode
- 80 ns

The SIMMs are 72-pin JEDEC standard. Many 72-pin SIMMs are 36 bits wide. This machine requires only 32 bits of data. If a 36-bit SIMM is used, then the extra 4 bits are simply ignored.

Fast RAM is controlled by the same RAMSEY chip used in the A3000. RAMSEY was designed to terminate cycles via *STERM. Since the 68020 only has *DSACKs, external logic is required to provide *DSACKs to the CPU in a synchronous fashion.

Burst mode is still functional for Fast RAM, but the 68020 does not have this capability. If a 68030 is installed in the coprocessor slot, it is desirable to have this turned on. Therefore, the test for static column DRAMs should be left in the ROM, and the BURST bit turned on just as is done with the A3000. However, the test for static column DRAMs must be done differently. Instead of writing four longwords with the static column bit set, and then reading them back with it off, the four longwords should be written with the bit set off, and then read back with it turned on. This is necessary because JEDEC standard SIMMs do not make use of an output enable (*OE) pin for the DRAMs. When static column mode is turned on, all writes to the DRAM are done as late writes. Without the *OE pin, the SIMMs cannot do late writes. The test will fail, indicating the correct result, but more significantly the data being written to the DRAMs will collide with data coming out of them, which is undesirable. Static column SIMMs must be custom made. One of the no connect pins will be assigned to act as the *OE pin. Only after it is determined that the DRAMs are the static column type should a write to DRAM in static column mode ever be allowed.

The test described above for static column DRAMS should not be done with a 68020. The software should check that the processor is a 68030 or 68040 before doing this test. Since the 68020 uses DSACK, this test will not perform properly.

If static column DRAMs are installed, page mode operation is functional as well (when the bit is turned on).

Table 6-1. Fast RAM Configurations

1 MB SIMM = 256K x 32/36
4 MB SIMM = 1M x 32/36

Table 6-2. Fast RAM SIMM Types

Total Fast RAM	Address	SIMM Configurations
1 Megabyte	07F00000-07FFFFFF	One 1 MB SIMM
2 Megabytes	07E00000-07FFFFFF	Two 1 MB SIMMs
3 Megabytes	07D00000-07FFFFFF	Three 1 MB SIMMs
4 Megabytes	07C00000-07FFFFFF	Four 1 MB SIMMs
8 Megabytes	07800000-07FFFFFF	Two 4 MB SIMMs
12 Megabytes	07400000-07FFFFFF	Three 4 MB SIMMs
16 Megabytes	07000000-07FFFFFF	Four 4 MB SIMMs

Chip RAM

- Up to 2 MB via one 72-pin SIMM
- 32-bit CPU interface
- 32/16-bit Chip interface
- Page or Static Column mode
- 80 ns

The base machine will contain 1 MB of Chip RAM, and is expandable up to 2 MB on the motherboard. The first 1 MB resides on the Chip RAM SIMM, configured as 256K x 32. If 2 megabytes of Chip RAM is desired, then this SIMM must be replaced with a single 512K x 32 SIMM.

The 2 MB of Chip RAM appears at 0000000-01FFFFF. Any uninstalled Chip RAM in this 2 MB will read back as 'garbage'.

Table 6-3. Chip RAM Configurations

Total Chip RAM	Configurations
1 Megabyte	One 256K x 32/36 SIMM
2 Megabytes	One 512K x 32/36 SIMM

ROM

Sockets are provided on the motherboard for two 128K x 16 ROMs. ROM appears at 0F80000-0FFFFFF. A jumper is provided on the motherboard to adjust ROM speed.

Table 6-4. ROM Jumper Settings

J0	CPU Cycles	Tacc
0	5	160 ns
1	6	200 ns

Since the same FAT GARY chip as in the A3000 is being used, some external logic was required to provide the required functionality. Since FAT GARY terminates ROM accesses with *STERM, an external PAL is required to convert this to synchronous *DSACKs for use with a 68020.

Writes to the ROM address range will cause a bus timeout to occur.

Real Time Clock

- Ricoh RTC with 26 x 4-bit battery backed RAM
- The A4000 uses the same Ricoh RTC as in the A3000

Floppy Disks

- One internal floppy drive standard (2 speed, high density, 1.7 MB)
- Up to two internal floppy drives (DF0: and DF1:)
- Up to two external floppy drives (DF2: and DF3:)

A single 1.7 MB internal floppy disk comes installed in the machine. The circuitry on the motherboard can support two internal drives. The standard disk is installed in the topmost drive bay, and uses the front bezel as its faceplate (32 mm or 25 mm). A second drive can be added in either of the lower two bays. Drives in these two bays require their own bezels. Also, the lowest bay is limited to a 25 mm drive only.

External drives (DF2: and DF3:) must be installed via the 23-pin external connector. A jumper is provided on the motherboard to redirect DF0: out the external connector. The first external drive would then be DF0:, and the second external drive would be DF3:.

The internal floppy connector is wired such that DF0: is connected before the twist in the floppy cable wire. DF1: would be after the twist.

Hard Disk

- Built in 16-bit IDE interface (internal connections only)
- Two drive support

An internal 40-pin connector is provided for the addition of up to two 16-bit AT IDE compatible hard disk drives.

Hard drives can be installed in two places. A single slim line (low profile) hard disk can be mounted in the lower bay of the bracket in the front of the machine (below the floppy). In addition, a single half height, or two low profile hard disks can be installed alongside the power supply in the back of the machine.

The IDE (AT) hard drive requires two mutually exclusive chip selects. Refer to the following tables for address range in which each is active. The state machine shown in Figure 6-2 is used for IDE accesses. Note that consecutive accesses cannot be performed nearly as fast as a single access. This would suggest that the optimum algorithm for access of IDE data would consist of single accesses of IDE data interleaved with single accesses of the target/source data buffer.

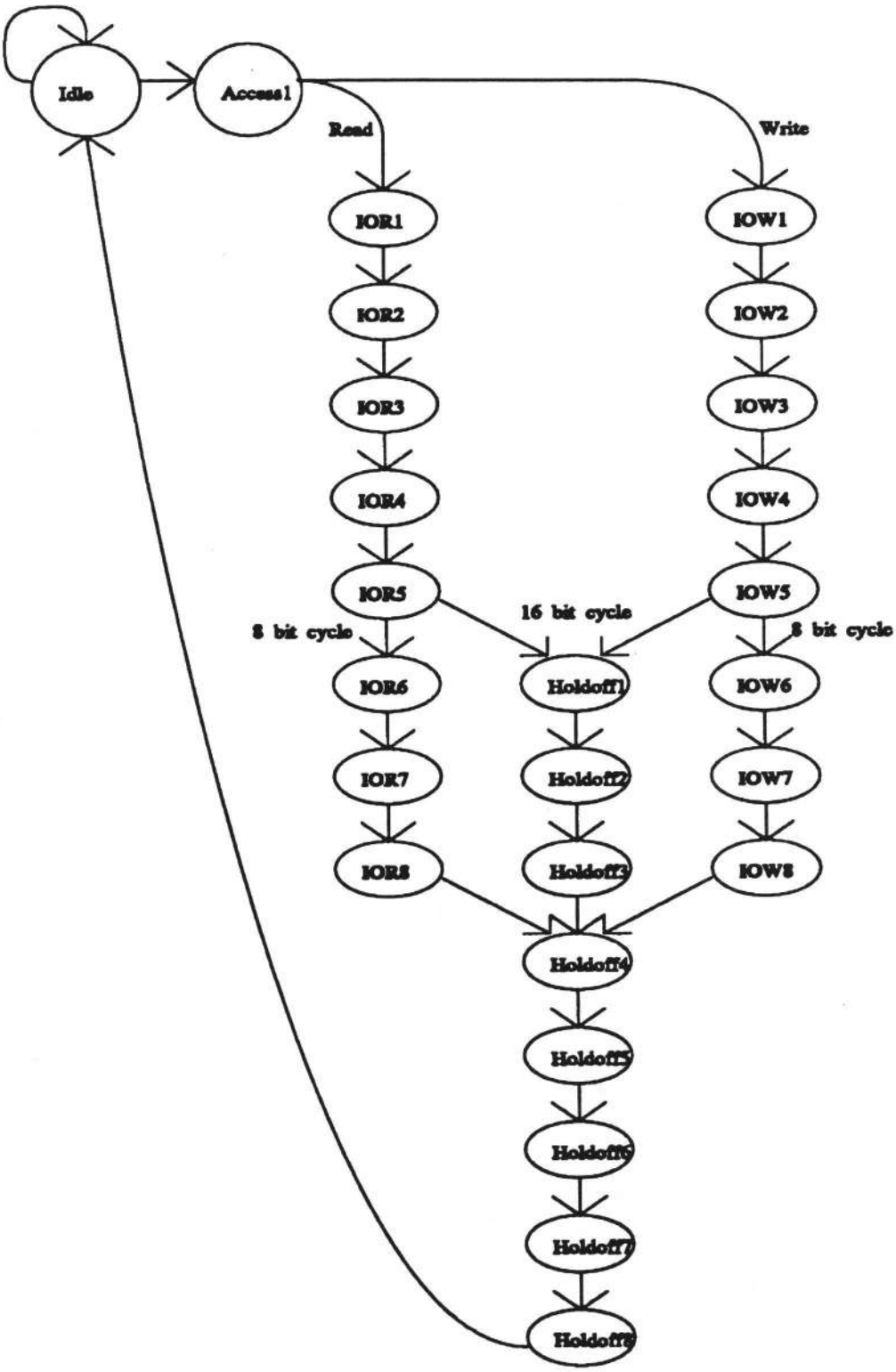


Figure 6-2. State Machine

Data register accesses can be performed faster than control register accesses. Accesses to the control registers are called "8-bit accesses" while those to the data register are called "16-bit accesses". Shown below is a table that gives addresses for all registers related to the IDE sub-system.

A13	A12	A5	A1	Address	Function
0	0	1	X	$0DD0XXX	Reserved for SCSI
0	1	1	0	$0DD1XX0	Reserved for mode register 0
0	1	1	1	$0DD1XX2	Reserved for mode register 1
1	0	1	0	$0DD2XX0	_CS1, 16-bit speed
1	0	1	1	$0DD2XX2	_CS1, 8-bit speed
1	1	1	0	$0DD3XX0	IDE interrupt register
1	1	1	1	$0DD3XX2	_CS2, 8-bit speed

Note that A5 must be high for all accesses. This is because contention with RAMSEY results if this is not done.

The A4000 supports four different timings. They represent reads and writes at 8-bit and 16-bit speeds. These timings are shown on the following pages.

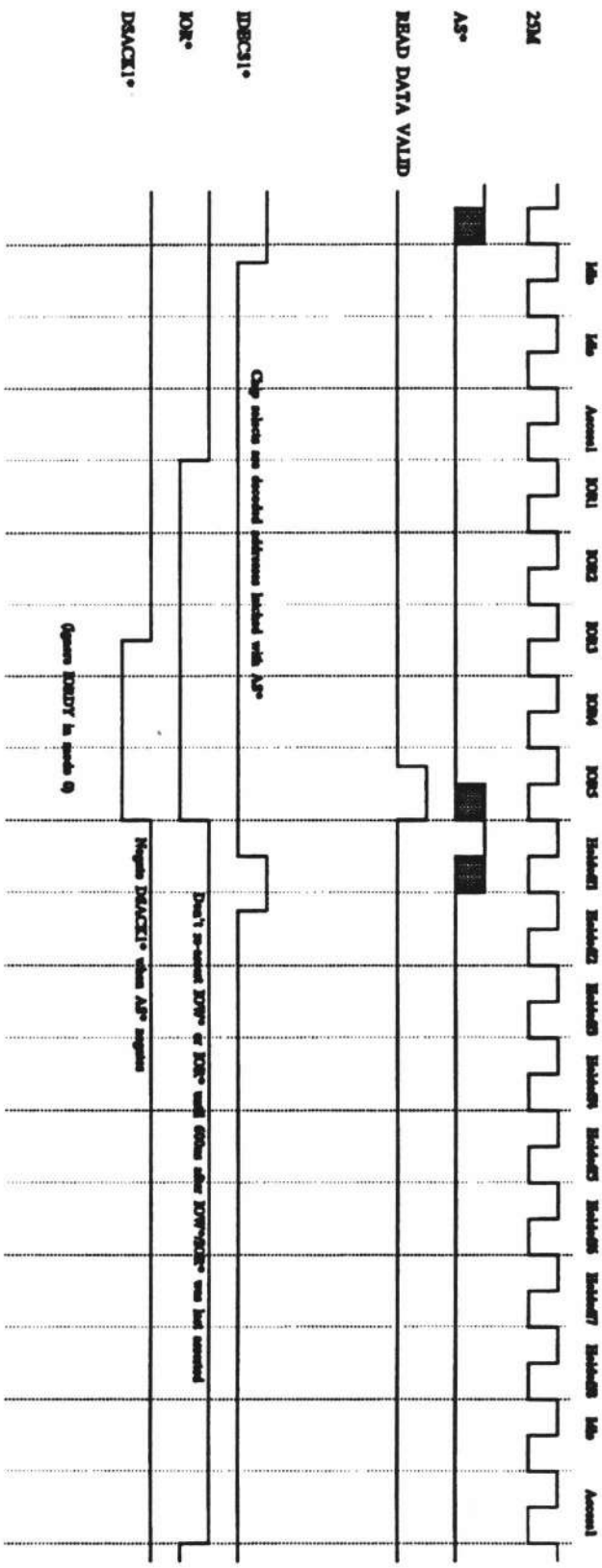


Figure 6-3. Timing Table 1

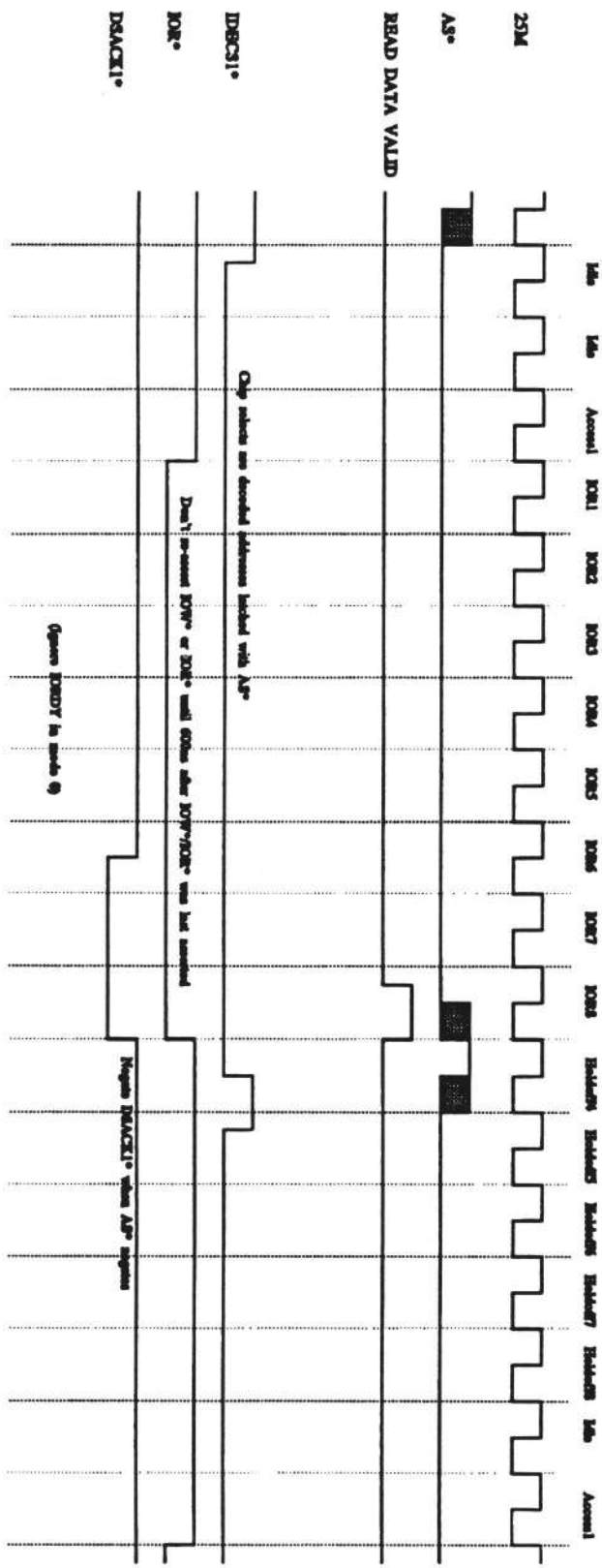


Figure 6-4. Timing Table 2

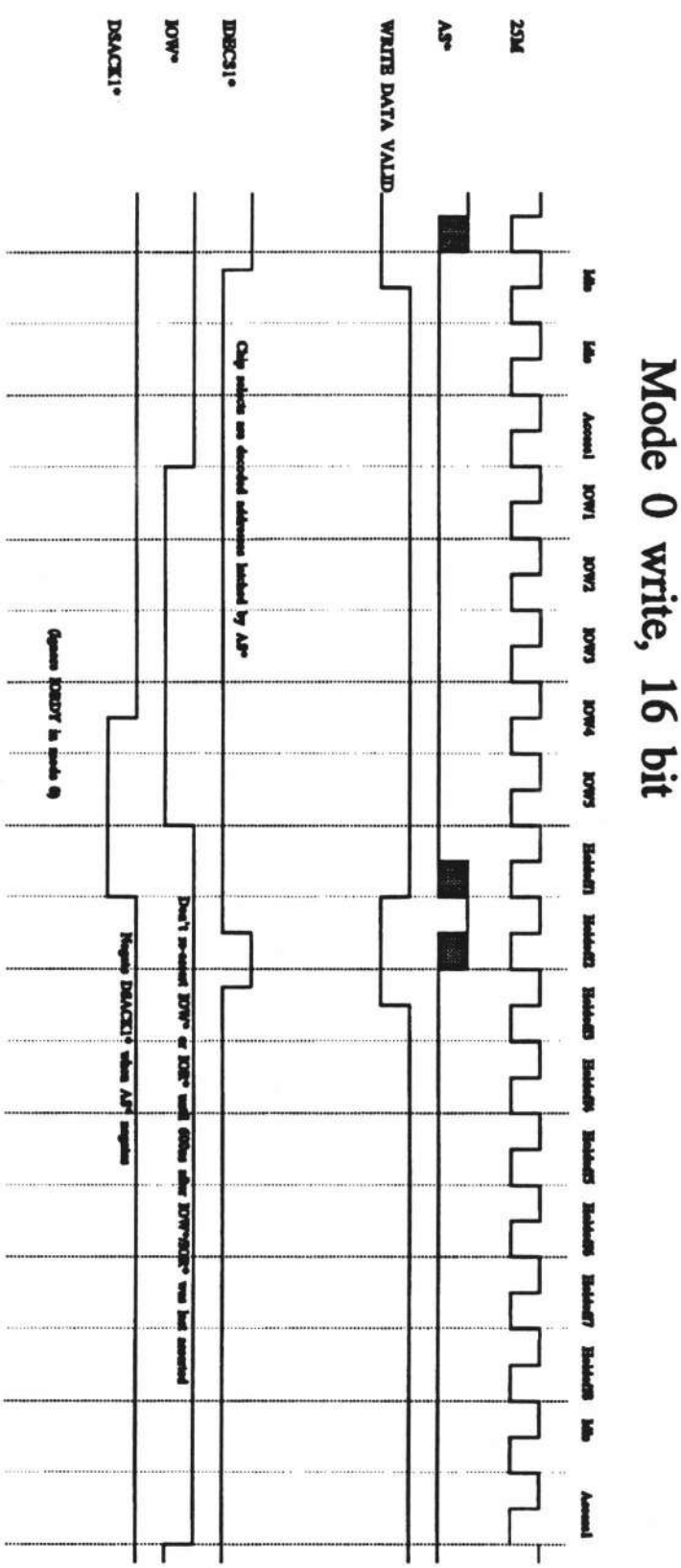


Figure 6-5. Timing Table 3

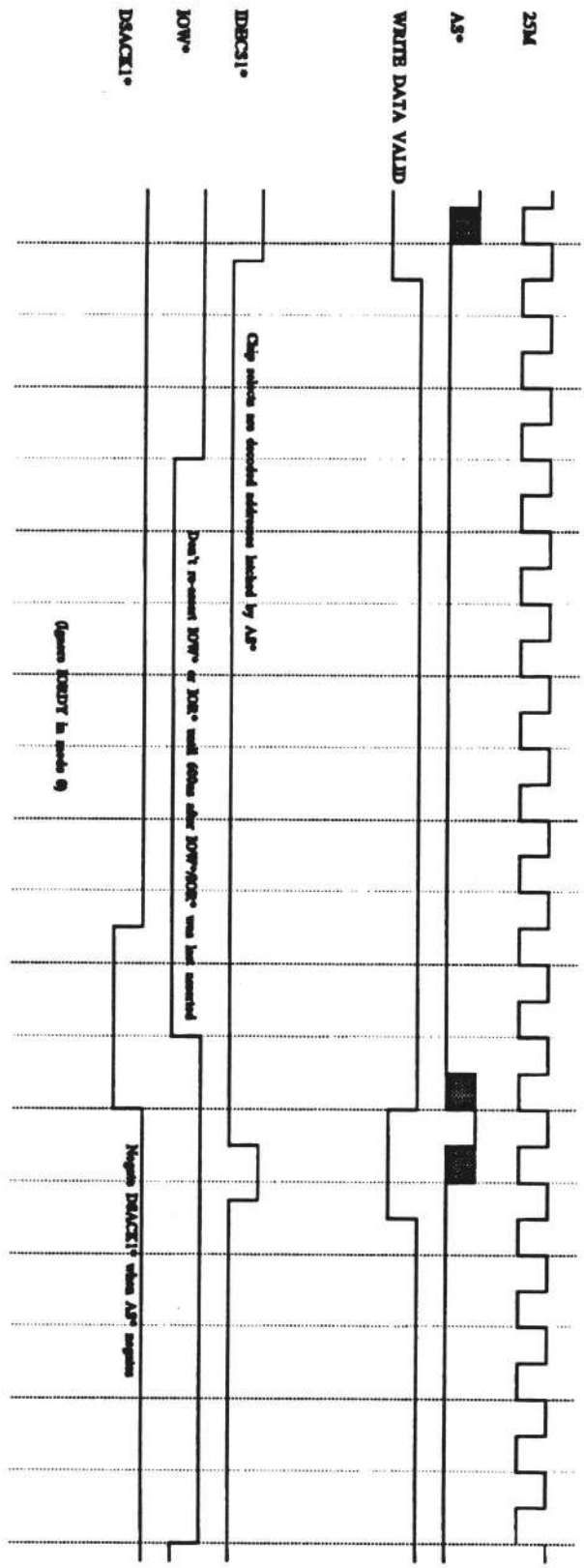


Figure 6-6. Timing Table 4

The disk drive address lines DA0, DA1, and DA2 are connected to processor address lines A2, A3, and A4, respectively. This results in the following memory map.

A1000 Address	Addr on AT Address	Valid Data	Read Function	Write Function
$0DD1020	-	D31	None	Mode Reg0 (reserved)
$0DD1022	-	D31	None	Mode Reg1 (reserved)
$0DD3020	-	D31	IDE int reg	None
$0DD303A	3F6	8 bits	Alternate Status	Device Control
$0DD303E	3F7	8 bits	Drive address	Not used
$0DD2026	1F1	8 bits	Error Register	Features
$0DD202A	1F2	8 bits	Sector Count	Sector Count
$0DD202E	1F3	8 bits	Sector Number	Sector Number
$0DD2032	1F4	8 bits	Cylinder Low	Cylinder Low
$0DD2036	1F5	8 bits	Cylinder High	Cylinder High
$0DD203A	1F6	8 bits	Drive/Head	Drive/Head
$0DD203E	1F7	8 bits	Status	Command
$0DD2020	1F0	16 bits	Data	Data

Locations $0DD1020 and $0DD1022 are reserved for the mode registers. These are currently not implemented. When implemented, they will allow faster transfer rates from hard drives that support such rates. Part of the ID of a drive is information that allows the driver to decide which 'mode' is the fastest the drive supports. Modes are defined as follows.

Mode Reg1	Mode Reg0	Mode Type	Maximum Transfer Rate
0	0	mode 0	3.3 MB/sec
0	1	mode 1	5.2 MB/sec
1	0	mode 2	8.3 MB/sec
1	1	Undefined	Undefined

As currently implemented, only mode 0 is available.

Location $0DD3000 contains the IDE interrupt register. This register returns a value of 1 if an interrupt is pending from the IDE hard disk, and a value of 0 if an interrupt is not pending from this source. Writing to this register has no effect.

Audio

Two external RCA jacks are provided for stereo audio output (pre-amp levels). As in the A3000, right and left channels are shorted together to provide combined monoraul audio if only a single RCA plug is installed. Separate right and left stereo is provided when male RCA plugs are inserted into both of the RCA jacks.

External audio in is provided on pin 18 of the RS-232 DB25 connector. This audio is mixed into the right channel. Audio out is also provided on the DB25 connector on pin 11, which is sent from the left audio channel.

An internal connector on the PCB allows for additional Right and Left audio to be mixed in. This allows internal expansion devices (such as a DSP) to provide stereo audio as well.

Keyboard

- detachable
- full size with keypad

The same keyboard as is used with the A3000 will be used with one modification — a new connector (6-pin MINI DIN).

Expansion Slots

- four Zorro II/III expansion card slots
- video slot in line with one Zorro slot
- 200-pin processor connector

Four horizontal expansion card slots are provided. One slot (bottom) contains a 100-pin Zorro II/III compatible connector in line with the two connector video slot. The remaining three slots have both Zorro II/III and IBM AT connectors.

Video cards that were designed for the A2000 have certain limitations in this casework. In the A3000 we provided an adapter bracket that allowed boards designed for the A2000 video slot to be used in the A3000. It attached to the large flat metal bracket on the video card and allowed it to be connected to a standard expansion slot opening. In the A4000, however, there is not enough room for the old bracket to remain (it sticks out the side of the box). Consequently, the old video slot bracket must be removed from the video card, and a new 'custom' bracket installed. This bracket is custom to each video card, and must be provided by each of the separate manufacturers since the location of the mounting holes is not standard.

A 200-pin KEL connector is provided on the motherboard which provides direct access to the processor bus signals. This connector is physically and electrically compatible with the coprocessor slot of the A3000. The board area available, however, is significantly smaller.

Since no processor exists on the motherboard of the A4000, this processor slot must be occupied by a CPU card for the machine to function. However, different CPU cards can be plugged into this slot in order to alter or enhance the system (such as future processors, or coprocessors).

Memory Map

00000000-001FFFFF	2 MB	Chip RAM (ROM at 0F80000 gets mapped to 0000000-0FFFFFF during overlay)
00200000-009FFFFF	8 MB	Zorro II expansion space
00A00000-00BFFFFF	1.5 MB	Zorro II expansion space
00B80000-00BFCFFF	448 KB	not used
00BFD000-00BFDFFF	4 KB	CIA #1
00BFE000-00BFEFFF	4 KB	CIA #0
00BFF000-00BFFFFF	4 KB	
00C00000-00CFFFFF	1 MB	Chip register shadow
00D00000-00D9FFFF	640 KB	unused
00DA0000-00DAFFFF	64 KB	
00DB0000-00DBFFFF	64 KB	unused
00DC0000-00DCFFFF	64 KB	Real-time clock
00DD0000-00DD0FFF	4 KB	reserved (SCSI)
00DD1000-00DD3FFF	12 KB	IDE registers

00DD4000-00DDFFFF	48 KB	unused
00DE0000-00DE7FFF	32 KB	RAMSEY/GARY registers (supervisor space)
00DE8000-00DEFFFF	32 KB	unused
00DF0000-00DF7FFF	32 KB	unused
00DF8000-00DFBFFF	16 KB	Auxilliary interrupt control
00DFC000-00DFFFFF	16 KB	Chip registers
00E00000-00E7FFFF	512 KB	reserved (System ROM expansion)
00E80000-00E8FFFF	64 KB	Zorro II autoconfig space
00E90000-00EFFFFF	512 KB	Zorro II I/O space
00F00000-00F7FFFF	512 KB	Cartridge space
00F80000-00FFFFFF	512 KB	System ROM
01000000-017FFFFF	8 MB	reserved (Chip RAM expansion)
01800000-06FFFFFF	88 MB	reserved (motherboard Fast RAM expansion)
07000000-07FFFFFF	16 MB	motherboard Fast RAM
08000000-0FFFFFFF	128 MB	coprocessor slot expansion
10000000-7FFFFFFF	(~2 GB)	Zorro III expansion space
80000000-FEFFFFFF	(~2 GB)	reserved
FF000000-FF00FFFF	64 KB	Zorro III autoconfig space
FF010000-FFFFFFFF		reserved

Casework

Basically, the casework is the same as the desktop PC compatibles. A different front bezel with a single molded floppy 'face' is required. Also, the internal floppy bracket is unique to properly line up the floppy with the new bezel.

Table 6-5. External Port Connections

External floppy	DB23M	rear
Parallel port	DB25F	rear (stacked)
Serial port	DB25M	rear (stacked)
Video	DB23F	rear
Keyboard	6-pin mini DIN	rear
Mouse/joysticks	two DB9	side (unstacked)
R/L audio	two RCA jacks	rear (unstacked)
Option plate	screw in plate	rear

Power Supply

A custom power supply is needed to meet the shape requirements of the case. The power supply requirements are as follows:

- +5 20.0 amps
- +12 4.0 amps (8A surge)
- -12 600 milliamps

The -12 capacity has been increased from the original PC specification (up from 300 to 600 mA) so that -5 (up to 200 mA) can be created on the motherboard with a -5 volt regulator.

The power supply will shut down if significantly more than the rated current is drawn from any of the voltages. Therefore, user voltages available at some of the external connectors are protected. However, since more than 8 amps is available from the power supply for +5, the +5 available at external connectors is current limited by a polyswitch 'fuse'. The polyswitches act like circuit breakers that open up when their maximum rating is exceeded. When the load is removed, they will automatically reset (after cooling off, which may take 30 seconds or more).

The 50/60 Hz TICK signal used in past Amigas has been generated in the power supply. However, the PC power supply does not have this capability. Therefore, the 8520 counter is connected to the Vertical Sync signal (as was done in the A500).

Refer to Power Supply specification 391173.

ASICs

BRIDGETTE

This is a new Gate Array which replaces the following TTL chips:

- Six 74F646s
- Four 74F245s

This results in reduced cost (~$10.00), reduced real estate and easier routing. BRIDGETTE can be used unchanged for the A3000 and other ECS/AA designs.

BRIDGETTE was done with NCR's technology and processing. This was necessary for two reasons — pin count and speed.

See *BRIDGETTE Chip Specification* on page 6-16.

FAT RAMSEY

RAMSEY is the Fast RAM controller that was designed for the A3000. It can be used for the A4000 with the addition of the following:

- One 16R4-10: *STERM to *DSACK conversion

See *RAMSEY Chip Specification* on page 6-29.

BUSTER

BUSTER can be used in the same fashion as in the A3000, and does not require any additional logic. See *BUSTER Chip Specification* on page 6-43.

FAT GARY

FAT GARY is a large 'glue' chip designed for the A3000 which performs a variety of tasks. It can be used in the A4000 with the addition of the following:

- One 6R4-10: *STERM to *DSACK conversion

See *FAT GARY Chip Specification* on page 6-45.

BRIDGETTE Chip Specification

Description

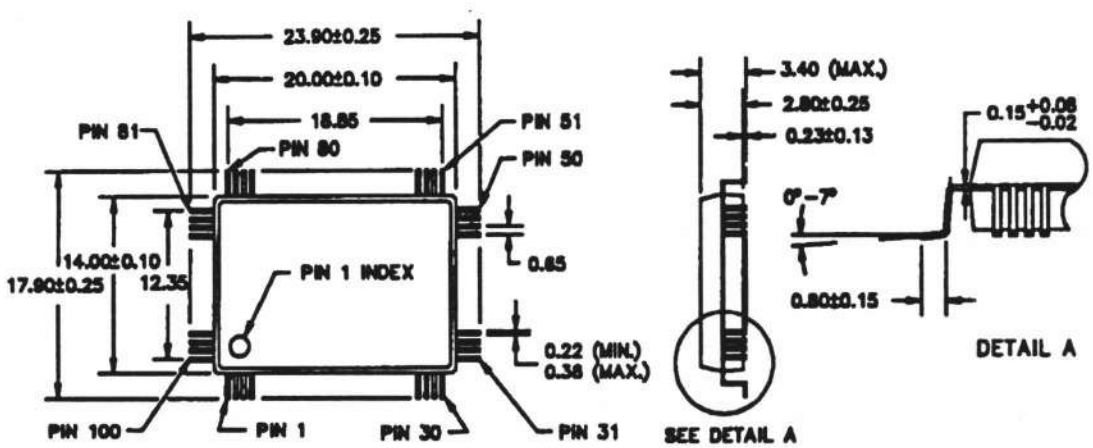
BRIDGETTE is a custom gate array IC designed for use in a wide range of Amiga computers. It implements data path routing and buffering necessary in any 68020/68030/68040 Amiga, as well as 68000 based Amigas with the AA chip set. The BRIDGETTE IC is a direct plug-in replacement for the data path buffers in the A3000. BRIDGETTE is packaged in a 100-pin Plastic Quad Flat Pack (PQFP) and provides the following functions:

- Data path (including latching) between the processor bus and chip bus
- Data path (including latching) between the processor bus and the expansion bus
- Bridging of the chip bus

Use of BRIDGETTE in a system represents a significant cost reduction over using separate TTL parts, as well as a reduction of real estate and routing complexity.

Configuration

The device shall be configured as a standard 100-pin Plastic Quad Flat Pack (PQFP) with external dimensions as shown in Figure 6-7.



NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL.
3. WHEN CONVERTING FROM MILLIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY.

Figure 6-7. Package Dimensions

Sources

Refer to *Approved Vendor List* on page 6-58.

Applicable Documents

Commodore Engineering Policy 1.02.007	Integrated Circuit Qualification Procedure
Commodore Engineering Policy 1.02.008	Integrated Circuit Process Test Specification

Pin Descriptions

Group	Name	Dir	Description
Common	PD0-PD31	Bi	Processor data bus.
	CD0-CD31	Bi	Custom chip data bus.
	XD0-XD15	Bi	Expansion bus data bus.
Chip Bridge	CBR	Input	Signal that enables bridging of CD0-CD15 and CD16-CD31.
	CBR_DIR	Input	Determines direction that chip data bus bridge is pointing. When this signal is high, data travels from CD16-CD31 to CD0-CD15. When low, data travels from CD0-CD15 to CD16-CD31.
PD to XD	_XOEL	Input	Output enable the path between PD0-PD15 and XD0-XD15.
	_XOEH	Input	Output enable for the path between PD16-PD31 and XD0-XD15.
	XDIR	Input	Direction control for the data path between PD and XD. When low, data travels from XD to PD. When high, data travels from PD to XD.
	XSTORED	Input	When the latch/buffer between PD16-PD31 and XD0-XD15 is set up so that data is travelling from XD to PD (XDIR low), this signal selects whether stored or real-time data is output on PD16-PD31. If XSTORED is low, real-time data is output. If high, stored data is output.
	XCLK	Input	On the rising edge of XCLK, data on XD0-XD15 is clocked in, for possible later output on PD16-PD31, as described above.
CD to PD	CDIR	Input	Direction control for the buffer/latch between the chip bus and processor bus. When low, data travels from the processor bus to the chip bus. When high, data travels from the chip bus to the processor bus.
	_COE	Input	Output enable for the path between the chip bus and the processor bus. If these buffers are pointing towards the CD bus, outputs are only enabled on the word of CD which the chip bridge is not pointing to, if the chip bridge buffer is enabled. If these buffers are pointing towards the PD bus, outputs are only enabled on the word of PD which a processor bridge is not pointing to, if any processor bridge buffers are enabled.
	_CLATCH	Input	This signal determines whether the data that the processor bus sees is real-time or latched chip bus data. If this signal is high, the data is real-time, if low the data is latched.

DC Characteristics

All specifications below are met over temperatures from 0 to 70° C, and supply voltages of 4.5 to 5.5 volts.

Pins	Parameter	Limits		Units
		MIN	MAX	
All but _XOEH	VIH	2.0		V
All but _XOEH	VIL	0.8		V
_XOEH	VIH (VCC = 4.5V)	3.15		V
_XOEH	VIH (VCC = 5.5V)	3.85		V
_XOEH	VIL (VCC = 4.5V)		1.35	V
_XOEH	VIL (VCC = 5.5V)		1.65	V
XD0-XD15	IOL (V = 0.5 max)	16		mA
XD0-XD15	IOH (V = 2.5 min)	16		mA
CD0-CD31	IOL (V = 0.5 max)	4		mA
CD0-CD31	IOH (V = 2.5 min)	4		mA
PD0-PD31	IOL (V = 0.5 max)	4		mA
PD0-PD31	IOH (V = 2.5 min)	4		mA
XD0-XD15	Load capacitance	100		pF
CD0-CD31	Load capacitance	50		pF
PD0-PD31	Load capacitance	50		pF

Data Paths

BRIDGETTE functionally emulates the TTL circuit displayed in Figure 6-8.

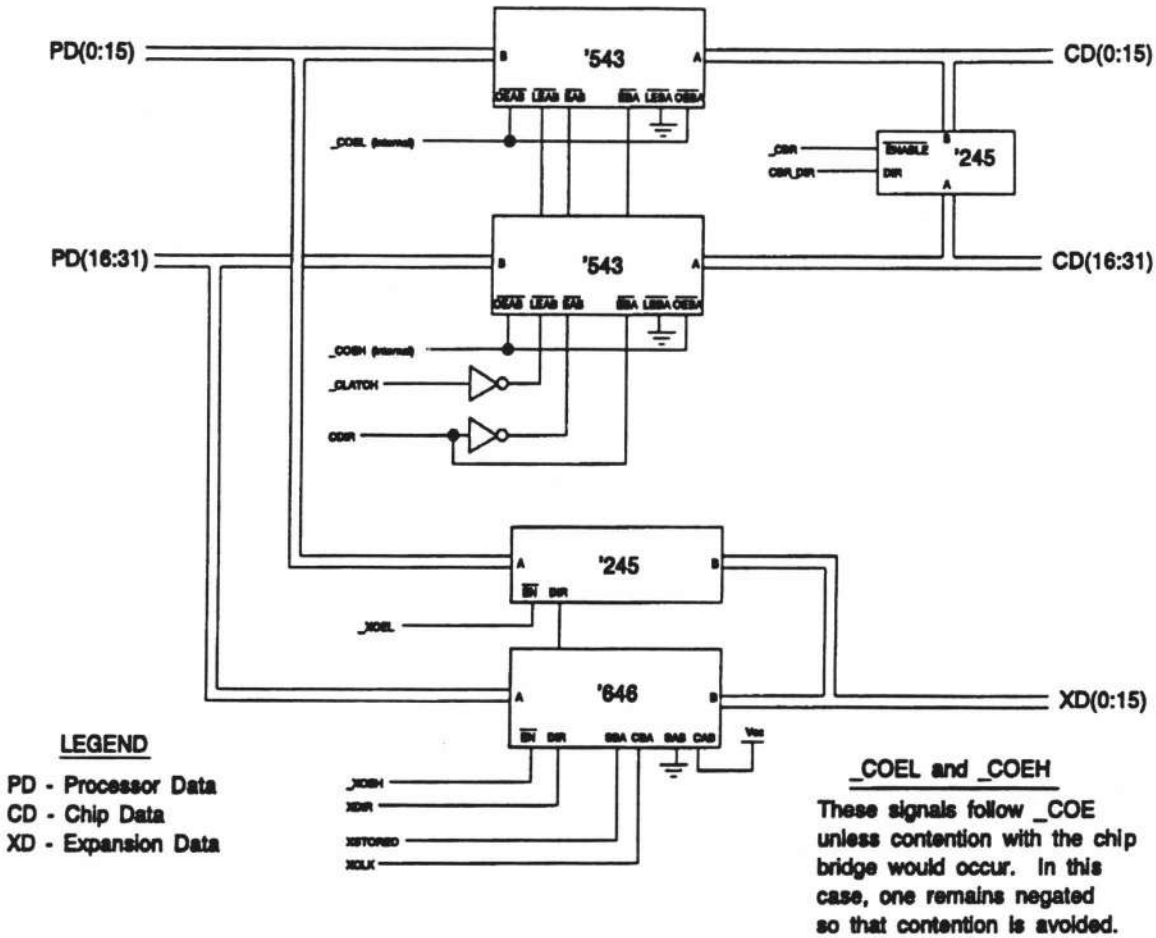


Figure 6-8. TTL Circuit

Chip Bridge Path

Data path

The data path referred to as "the chip bridge path" is shown in Figure 6-9.

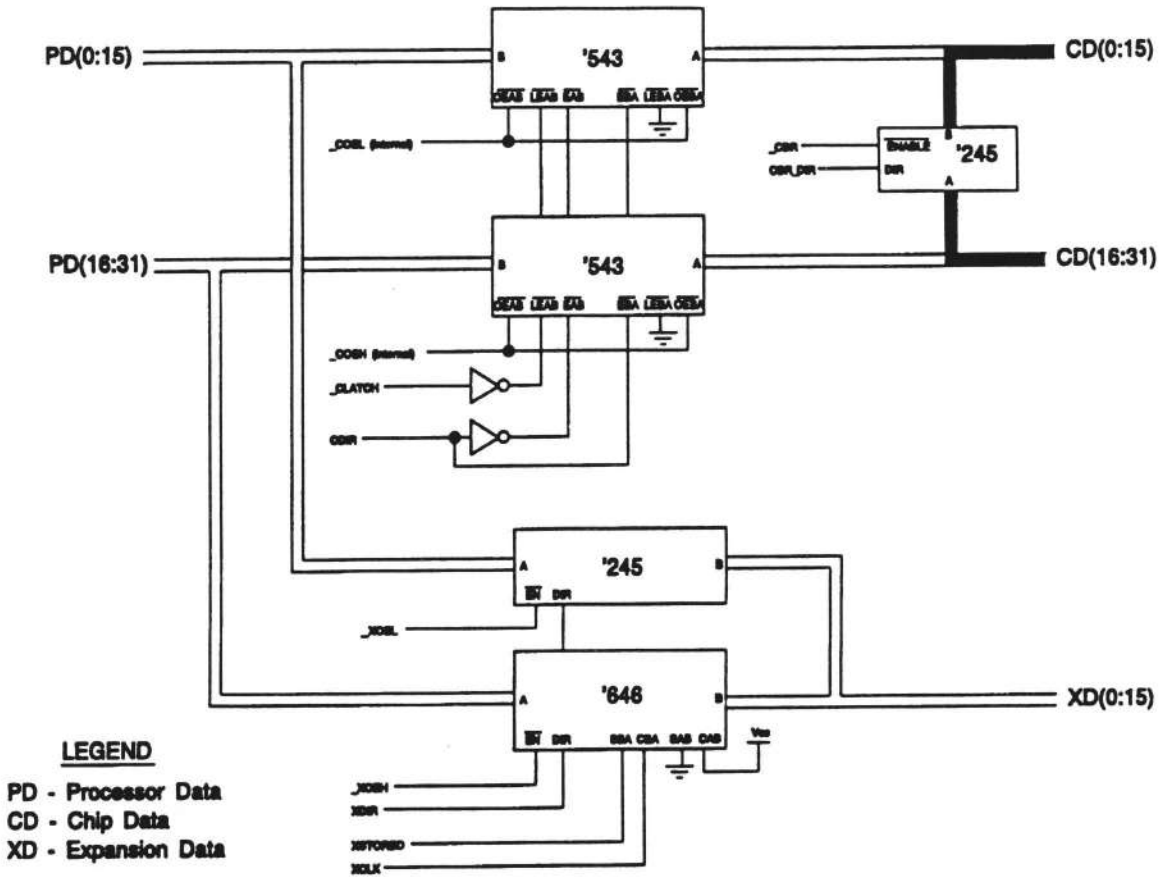


Figure 6-9. The Chip Bridge Path

Truth Table

The truth table for the chip bridge path is shown below.

Inputs		Output
_CBR	CBR_DIR	
L	L	CD(0:15) to CD(16:31)
L	H	CD(16:31) to CD(0:15)
H	X	High Z State

Timing

Timing specifications for this path are shown below. In all cases, timings shown are worst case, over full rated temperature and voltage.

Propagation delay, CD(16:31) to CD(0:15) or CD(0:15) to CD(16:31)	13.1 ns max
Output enable time, _CBR to data valid	17.4 ns max
Output disable time, _CBR to data high Z	9.4 ns max
Direction change time, CBR_DIR to data valid	17.8 ns max

Processor to Chip Data Path

Data Path

There are two paths included in this section. Most cases refer to the path displayed in Figure 6-10.

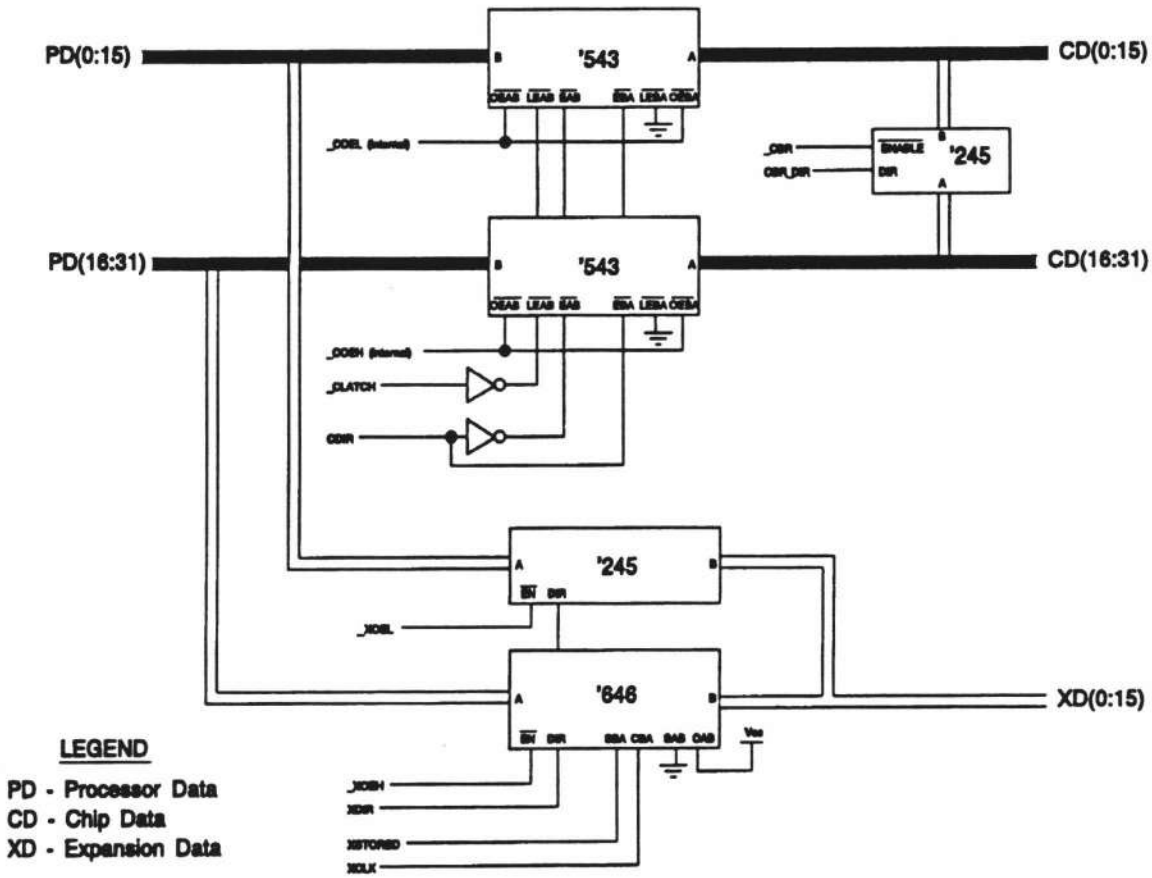


Figure 6-10. Data Path 1

The two cases shown in the second truth table where CDIR, _COE, and _CBR are low refer to the path displayed in Figure 6-11.

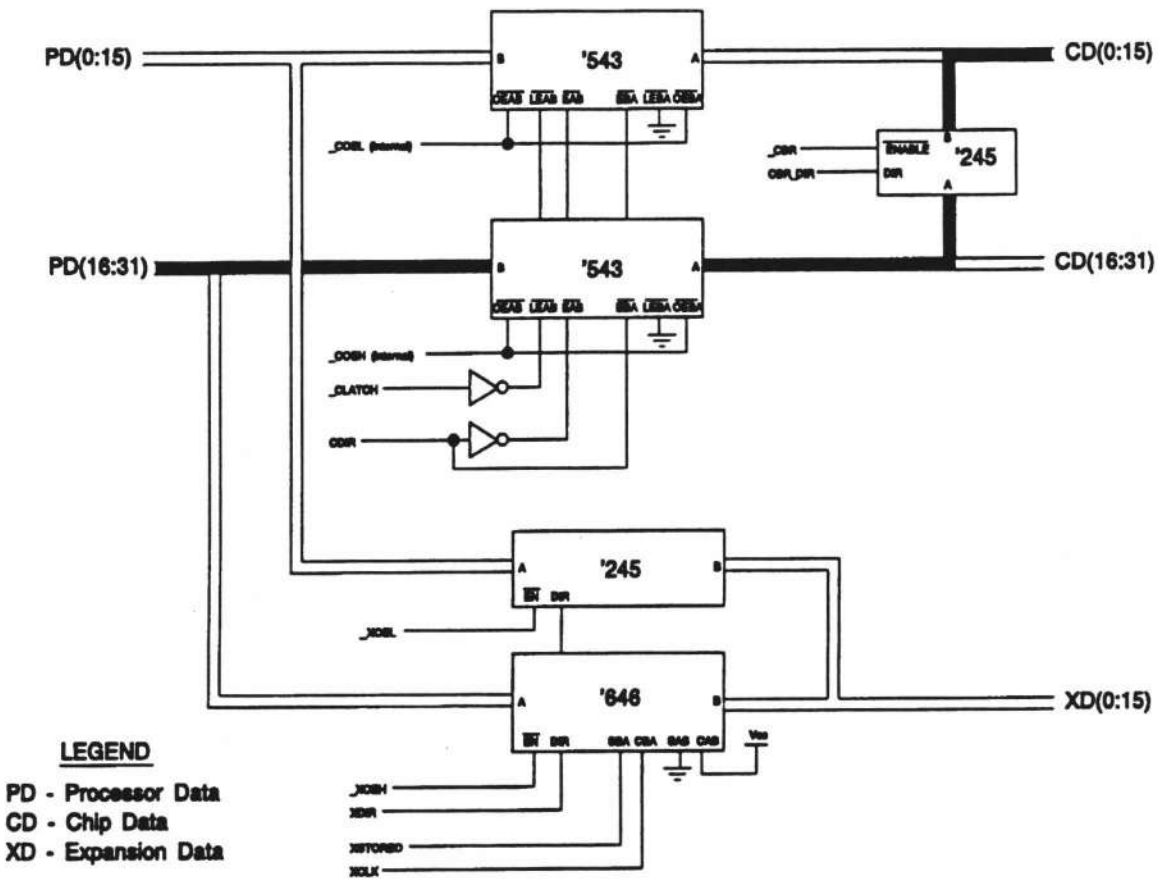


Figure 6-11. Data Path 2

Truth Tables

The truth tables for the processor to chip data path are shown below.

Inputs			Latch Status	Output Buffers
CDIR	_CLATCH	_COE	CD to PD	PD(0:31)
L	X	X	Storing	High Z
X	L		Storing	--
X		H	--	High Z
H	H	L	Transparent	Current CD inputs
H	L	L	Storing	Previous CD inputs

Inputs				Output Buffers	
CDIR	_COE	CBR	CBR_DIR	CD(0:15)	CD(16:31)
H	X	X	X	High Z	High Z
X	H	X	X	High Z	High Z
L	L	H	X	PD(0:15)	PD(16:31)
L	L	L	H	PD(16:31)	PD(16:31)
L	L	L	L	PD(0:15)	PD(0:15)

Timing

Timing specifications for this path are shown below. In all cases, timings shown are worst case, over full rated temperature and voltage.

Propagation delay, transparent mode, CD0-CD31 to PD0-PD31	15.6 ns max
Propagation delay, transparent mode, PD0-PD31 to CD0-CD31	13.2 ns max
Propagation delay, CD0-CD15 to PD16-PD31	26.3 ns max
Propagation delay, PD16-PD31 to CD0-CD15	28.7 ns max
Output enable time, _COE to data valid	17.4 ns max
Output disable time, _COE to data high Z	9.4 ns max
Setup time, CD to _CLATCH low	0 ns min
Hold time, _CLATCH low to data changing	3 ns min

Upper Processor Data to Expansion Data Path

Data Path

The data path referred to as the "upper processor data to expansion data path" is shown in Figure 6-12.

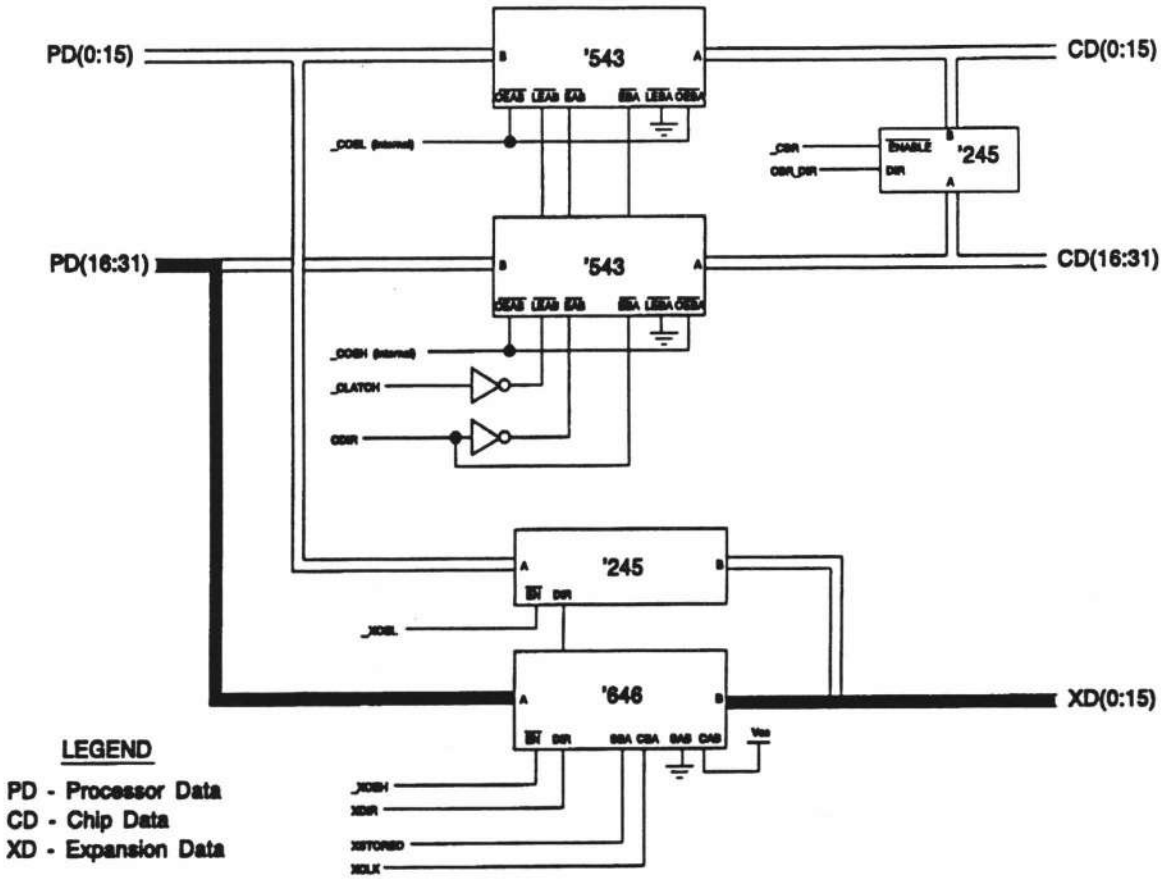


Figure 6-12. Upper Processor Data to Expansion Data Path

Truth Table

The truth table for this data path is shown below.

Inputs				Data I/O		Operation or Function
_XOEH	XDIR	_XCLK	XSTORED	PD(16:31)	XD(0:15)	
H	X	H or L	X	Input	Input	Isolation
H	X	Rising	X	Input	Input	Store XD
L	L	X	L	Output	Input	Real-time XD to PD
L	L	X	H	Output	Input	Stored XD to PD
L	H	X	X	Input	Output	Real-time PD to XD

Timing

Timing specifications for this path are shown below. In all cases, timings shown are worst case, over full rated temperature and voltage.

Propagation delay, PD to XD	11.4 ns max
Propagation delay, XD to PD	13.6 ns max
Output enable time, _XOEH to PD data valid	17.1 ns max
Output enable time, _XOEH to XD data valid	10.3 ns max
Output disable time, _XOEH to PD data high Z	5.8 ns max
Output disable time, _XOEH to XD data high Z	8.9 ns max
Data direction time, XDIR falling to PD data valid	19.1 ns max
Data direction time, XDIR rising to XD data valid	22.6 ns max
Setup time, XD to XCLK rising	0 ns min
Hold time, XCLK rising to data changing	2 ns min

Lower Processor Data to Expansion Data Path

Data Path

The data path referred to as "the lower processor data to expansion data path" is shown in Figure 6-13.

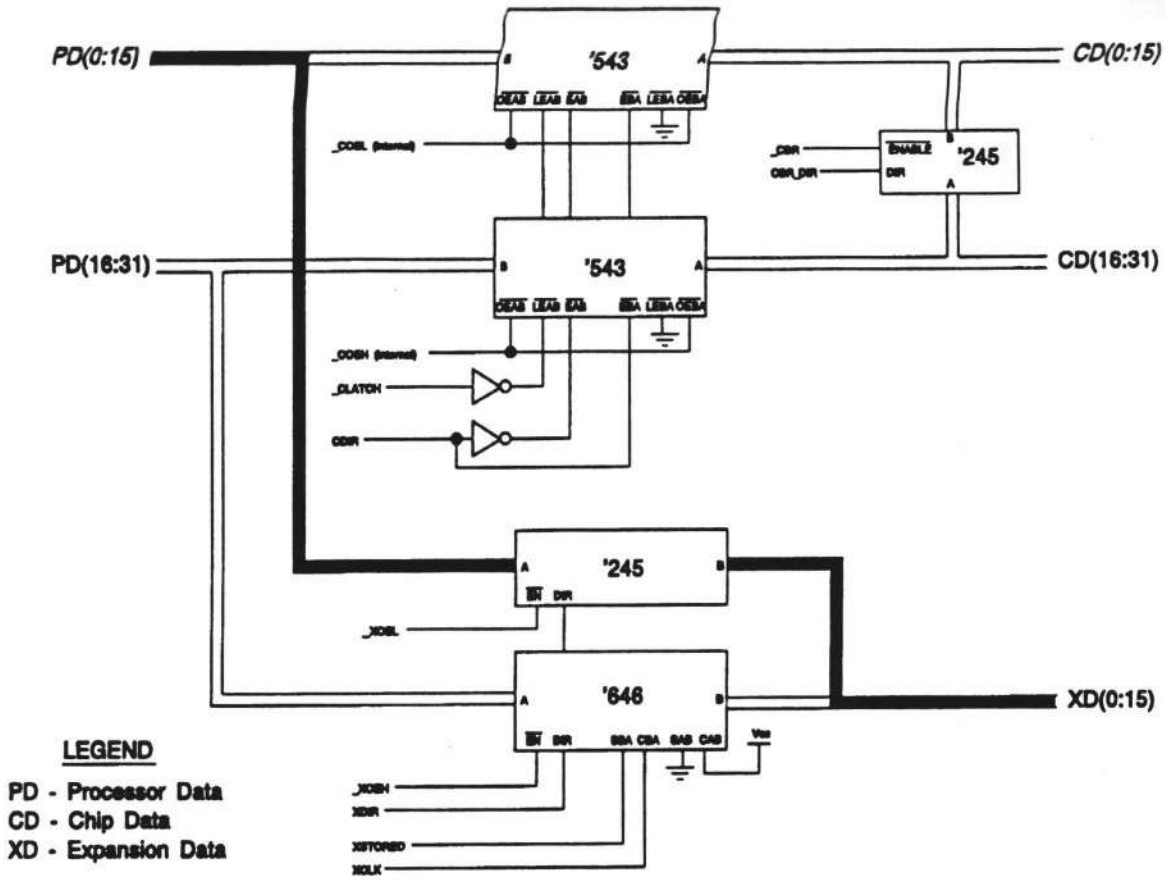


Figure 6-13. The Lower Processor Data to Expansion Data Path

Truth Table

The truth table for the lower processor data to expansion data path is shown below.

Inputs		Output
XOEL	**XDIR**	
L	L	XD(0:15) to PD(0:15)
L	H	PD(0:15) to XD(0:15)
H	X	High Z State

Timing

Timing specifications for this path are shown below. In all cases, timings shown are worst case, over full rated temperature and voltage.

Propagation delay, XD(0:15) to PD(0:15)	13.4 ns max
Propagation delay, PD(0:15) to XD(0:15)	11.4 ns max
Output enable time, _XOEL to XD data valid	13.4 ns max
Output enable time, _XOEL to PD data valid	18.1 ns max
Output disable time, _XOEL to XD data high Z	9.0 ns max
Output disable time, _XOEL to PD data high Z	10.4 ns max
Direction change time, XDIR falling to PD data valid	21.8 ns max
Direction change time, XDIR rising to XD data valid	22.6 ns max

Physical Requirements

Marking

Parts shall be marked with Manufacturer's Part Number, Manufacturer's Identification, and EIA Date Code.

Packaging

The interconnected logic circuitry shall be contained in a 100-pin PQFP plastic package with exterior dimensions per Figure 6-7.

Environmental Requirements

Units furnished to the requirements of this specification shall meet the following environmental resistance requirements (vendors shall furnish supporting documentation upon request).

Operating Temperature	0 to 70° C
Operating Humidity	5 to 95% RH non-condensing
Operating Altitude	0 to 3000 meters
Storage Temperature	- 20 to + 85° C
Storage Humidity	5 to 95% RH non-condensing
Storage Altitude	0 to 15,000 meters

Process Qualification Tests

Integrated circuits supplied to the requirements of this specification shall meet the requirements of Engineering Policy No. 1.02.008. Supporting documentation shall be supplied by vendor upon request.

Environmental Test Conditions

Devices shall comply with the following environmental resistance tests per Commodore Engineering Policy 1.02.007.

1. Temperature/humidity (85° C and 95% RH non-condensing) for 168 hours
2. Operating life (1000 hours at 70° C ambient temperature)
3. Solderability per MIL-STD-883, Method 2003
4. Pressure cooker (15 psig, 120° C, and 100% RH for 24 hours)
5. Solvent resistance per MIL-STD-883, Method 2015, using water and trichloroethane
6. Solder temperature resistance (250° C for five seconds)
7. ESD requirement MIL-STD 1686 Group 3

Note: Devices shall meet this specification's operating performance requirements after the above tests are completed.

Minimum Acceptance Level

The minimum acceptance level of any lot shall be an AQL of 0.65 as defined by MIL-STD 105 single sampling techniques.

Age of Devices

Unit shall be rejected if EIA Date Code indicates an age of three (3) or more years.

RAMSEY Chip Specification

Description

This specification describes the requirements for an integrated circuit which is a custom gate array designed to function mainly as a dynamic RAM controller. The device, called RAMSEY, allows the 68030 chip to interface with up to 16 megabytes of system DRAM. RAMSEY also contains logic associated with the DMAC controller (super DMAC).

Some of the key features of RAMSEY are:

- Four megabytes of memory using 32 standard 256K x 4 DRAMs (80 ns)
- Sixteen megabytes of memory using 32 standard 1M x 4 DRAMs (80 ns)
- Support of 68030 burst mode (requires 80 ns static column DRAMs)
- Page mode RAM access (requires 80 ns static column DRAMs)
- Automatic CAS-before-RAS refreshing of DRAMs
- Multiplexing of addresses

Configuration

The device shall be configured as a standard 84-pin PLCC. Refer to Figure 6-14 for pin configuration. Refer to Figures 6-15 through 6-20 for timing diagrams.

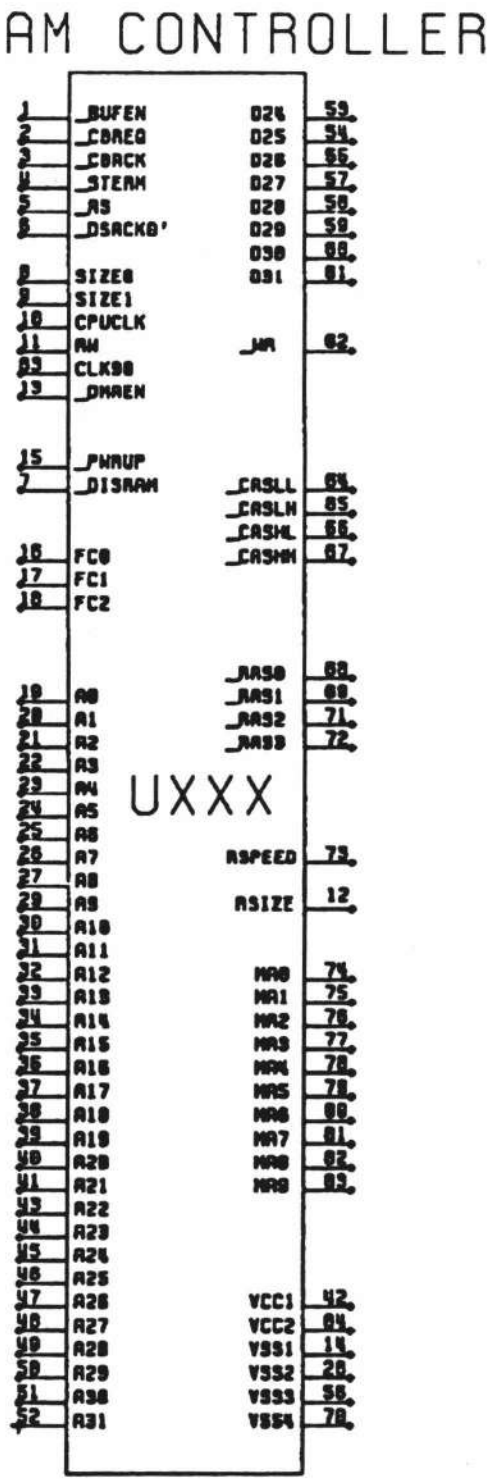


Figure 6-14. Pin Configuration

Sources

Refer to *Approved Vendors List* on page 6-58.

Pin Description

Name	Dir	Description
D24-D31	Bi	Data signals from/to 68030.
A0-A31	Bi	Address inputs from 68030. Become outputs when *DMAEN is valid.
FC0-FC2	Bi	Function code inputs from 68030. Outputs when *DMAEN is valid.
RW	Bi	Read/write input from 68030. Output when *DMAEN is valid.
SIZE0,1	Bi	Function code inputs from 68030. Outputs when *DMAEN is valid.
*AS	Input	Address strobe input.
CBREQ	Input	Cache burst request from 68030.
*CBACK	Output	Cache burst acknowledge. Tri-state output that is turned on when the RAM address space is decoded.
*STERM	Bi	Synchronous termination. Output during RAM access. Input when *DMAEN is valid. Tri-state output that is turned on when the RAM address space is decoded.
*PWRUP	Input	Powerup input. When valid, the internal register is restored to its default values.
*DISRAM	Input	Disable RAM. When valid, internal decoding of the RAM address space is disabled.
*DMAEN	Input	DMA enable. Input from onboard DMAC indicating that it is now the bus master.
*DSACK0	Bi	Data size and acknowledge (bit 0) output to 68030 (open collector). Input when *DMAEN is valid.
CPUCLK	Input	System clock.
CLK90	Input	System clock delayed 90 degrees.
*BUFEN	Output	Buffer enable. Output enable signal for 74F245s which tie the local RAM data bus to the system's data bus.
*WR	Output	Write signal to the DRAMs.
*CASxx	Output	Column address strobes to the RAMs.
*RASx	Output	Row address strobes to the RAMs.
RSPEED	Input	RAM speed. When high, the RAM controller assumes a 25 MHz system. If low, assumes 16 MHz operation.
RSIZE	Input	RAM size. If low, assumes the RAMs are 256K x 4. If high, assumes they are 1M x 4.
MA0-MA9	Output	Multiplexed address bits to DRAMs.

Note For -07 only, the following pins have a TTL Vih min. of 2.4. These values supersede documents dated before March 17, 1992.

Signal Name	Pin	Signal Name	Pin
DISRAM_I_	7	RSIZE_I	12
SIZE1	9	OWN_	13
CPUCLK_I	10	CLK90_I	63
RW_1	11	SPEED	73

Operation

RAMSEY Control Register

There is a single 8-bit register internal to RAMSEY which can be used to change its mode of operation. This register is readable and writable. It is located at $00DE0003 of the supervisor data space. Data written into the register does not take effect until the next refresh occurs. Consequently, if you write a value to the register you will have to wait out the refresh interval before the value can be read back. Each of these bits has a default value that it is set to when the *PWRUP bit is low.

bit 0	Page Mode	When high, page mode is enabled (default=0).
bit 1	Burst Mode	When high, RAMSEY will respond to the *CBREQ input and do burst cycles (default=0).
bit 2	Wrap	If high, all 4 longwords of a burst will be allowed to take place. If Wrap is disabled, then the burst will only continue while A3,A2 are increasing. Bursts will not be allowed to wrap to A3,A2=00 (default=0).
bit 3	RAMsize	If low, then RAM is 1 megabit (256K x 4 or 1M x 1). If high, then RAM is 4 megabit (1M x 4). The default value is determined by the RSIZE input.
bit 4	RAMwidth	For -04 only, if low, then RAM is 1 bit wide (1M x 1). If high, then RAM is 4 bits wide (256K x 4 or 1M x 4) (default=1).
bit 4	Skip	For -07 only, if set high, then RAM is accessed in 4 clocks, instead of 5 (25 MHz). S11 in timing diagrams is omitted. This requires VERY fast DRAMs (default = 0).
bit 5,6	Refresh Rate	The refresh counter uses the CPUCLK to count out refresh times. The number of clocks between refreshes is determined by the following table:

		Refresh Interval (μsecs)	
Bit 6,5	# of Clocks	16 MHz	25 MHz
00	154	9.24	6.16
01	238	14.28	9.52
10	380	22.8	15.2
11	oo	(refresh turned off)	

Since 512 refreshes must be done in 8 msecs, the interval between refreshes must be less than 15.625 μsecs. During page mode, RAS can only be low for 10 μsecs at a time, so the refresh rate should be set to less than 10 μsecs when page mode is enabled. The default values are determined by the RSPEED input. If RSPEED is low, then the default value for bits 6,5=00. If RSPEED is high, then the default for bits 6,5=01.

bit 7 TEST This bit is used for testing only.

Version Register

There is a read only register at $00DE0043 that contains the version number of the RAMSEY chip.

-04 (12D) RAMSEY returns a version number of $0D.

-07 (12G) RAMSEY returns a version number of $0F.

RAM Memory Map

$07C00000 - $07CFFFFF	RAS0
$07D00000 - $07DFFFFF	RAS1
$07E00000 - $07EFFFFF	RAS2
$07F00000 - $07FFFFFF	RAS3

RSIZE=0, RAMWIDTH=1

$07000000 - $073FFFFF	RAS0
$07400000 - $077FFFFF	RAS1
$07800000 - $07BFFFFF	RAS2
$07C00000 - $07FFFFFF	RAS3

RSIZE=1, RAMWIDTH=1

$07C00000 - $07FFFFFF	RAS0

RSIZE=0, RAMWIDTH=0

RAM Controller Description

RAMSEY is designed to work at two system speeds: 16.67 MHz and 25 MHz. The RSPEED input tells RAMSEY which speed the system is using.

In an effort to improve overall system performance, RAMSEY has several different modes of operation. The two basic modes of operation are referred to as standard and page. Both standard and page modes can be run with or without burst mode, and burst mode can be done with or without burst wrap enabled.

Standard Mode

In this type of operation both page mode and burst mode are disabled. This mode requires standard 80 ns page mode DRAMs. Access to the RAMs always takes five cycles at 25 MHz and four cycles at 16 MHz.

Page Mode

This mode requires 80 ns static column mode DRAMs. When the RAM is accessed, RAS is held low after the cycle completes. This leaves the current RAM 'page' open. While RAS is low, the RAM behaves like a static RAM. Any data within the current page can be accessed by changing the column addresses only. Since the column access time (t_{AA}) is much less than the RAS access time (t_{RAC}), subsequent access to this page of data can be done faster. As long as RAS is held low (10 μsecs max) RAMSEY will allow the CPU to access RAM on this page in only three cycles (16 and 25 MHz).

Comparators inside RAMSEY monitor the ROW address of RAM accesses. If a page is currently open and the ROW address matches (page hit), the RAM can be read in three cycles. If the comparators detect that the data being requested is on a different page (page miss), then RAS must be cycled high and low again, opening up a new page in RAM. Since RAS must be cycled high when a page miss occurs, RAM access takes longer (seven cycles at 25 MHz, five at 16 MHz).

There is some difference in how page mode is done at 16 MHz versus 25 MHz. At 25 MHz, the page comparator only detects page misses when *AS is low and RAM is being accessed. Therefore, when a page is opened (RAS held low), it will remain open until the next refresh occurs, or a page miss is detected. At 16 MHz, however, the page comparator will detect a page miss while *AS is high. Therefore, at 16 MHz a page will only stay open as long as consecutive bus cycles access RAM in this page (or a refresh occurs). At 25 MHz the page will remain open even if bus cycles in between accesses to the currently opened page occur (such as chip memory, CIAs, etc.). This is done so that page misses at 16 MHz will only take five cycles — addresses are valid 1/2 cycle before *AS (30 ns). If it waited until *AS was valid before detecting a page miss, the RAS precharge requirement (t_{RP}) could not be met in 5 cycles.

Burst Mode

This mode requires 80 ns static column DRAMs. In this mode, RAMSEY will respond to the *CBREQ input from the 68030 and allow burst access to RAM. Burst cycles take two clocks each.

Burst Wrapping

The WRAP bit in the RAMSEY control register is associated with burst mode. The 68030 will always request four longword values during a burst sequence. However, if the initial longword is not aligned on a quad longword (A3,A2 not equal to 0,0), the 68030 will read in data which is behind the first data it asked for. Since it is less likely that this data will be used, the WRAP control bit allows you to prevent the 68030 from doing this. If WRAP is low, then the burst will stop after the data with A3,A2 = 1,1 is accessed. If WRAP is high, then all four longwords will be burst.

Since burst and page modes require the use of static column DRAMs, the system must have some means of determining which type of RAMs it contains. If page or burst modes are turned on 'blindly', the machine could crash. Each 1 megabyte bank of Fast memory must be checked. The proper method of checking for static column DRAMs is the following:

1. Disable all interrupts.
2. Turn page mode on by setting the bit in the RAMSEY control register (read it back until the bit takes effect).
3. Write $5AC35AC3, $AC35AC35, $C35AC35A, $35AC35AC to four consecutive longwords in the same page (to be in the same page, A11-A31 must be the same for all four longwords).
4. Turn page mode off by resetting the bit in RAMSEY (wait for it to take effect).

5. Compare the four longword values with what they were written with. If they are correct, then this bank of RAM has all static column DRAMs.
6. Repeat steps 2 through 5 for each 1 MB bank of Fast memory.
7. Re-enable interrupts.

The code that executes this test must **not** be in Fast RAM. Any access to Fast RAM with page mode turned on could cause corruption if any of the RAMs are not static column type. Also, since a refresh cycle will close the page, writes to the four longwords of RAM **must** be less than 10 μsecs apart.

DMAC Support

RAMSEY contains the address counters used during DMA via the onboard contoller. When *DMAEN becomes low, the address lines become outputs and provide the DMA addresses. The DMA address is incremented on the rising edge of *AS whenever *DMAEN is low. Since DMA to both 32 and 16-bit ports is supported, RAMSEY must monitor how the cycle was terminated so that it can increment the address counter by the appropriate amount. If *STERM transitioned low sometime during the cycle, then the port was 32 bits wide and the address is incremented by four. If *DSACK0 transitions during the DMA bus cycle, then the port was also 32 bits wide (*DSACK0 and *DSACK1 are both set low to terminate an asynchronous 32-bit transfer). If neither signal is seen to transition, then it can be assumed that the cycle was terminated by *DSACK1, indicating that the port was 16 bits wide, and the address is incremented by two.

The address counters are preset before DMA is done by writing to the 32-bit register at location $00DD000C (this register is readable as well). The counter can only be preset to a longword-aligned boundary (bits 1 and 0 are always written as 0,0).

-04 The counter can only be preset to an even longword boundary (bits 1 and 0 are always written as 0,0).

-07 The counter can only be preset to an even word boundary (bit 0 is always written as 0). If A1 is high when a cycle terminates, the address is always incremented by 2 regardless of how the cycle terminates.

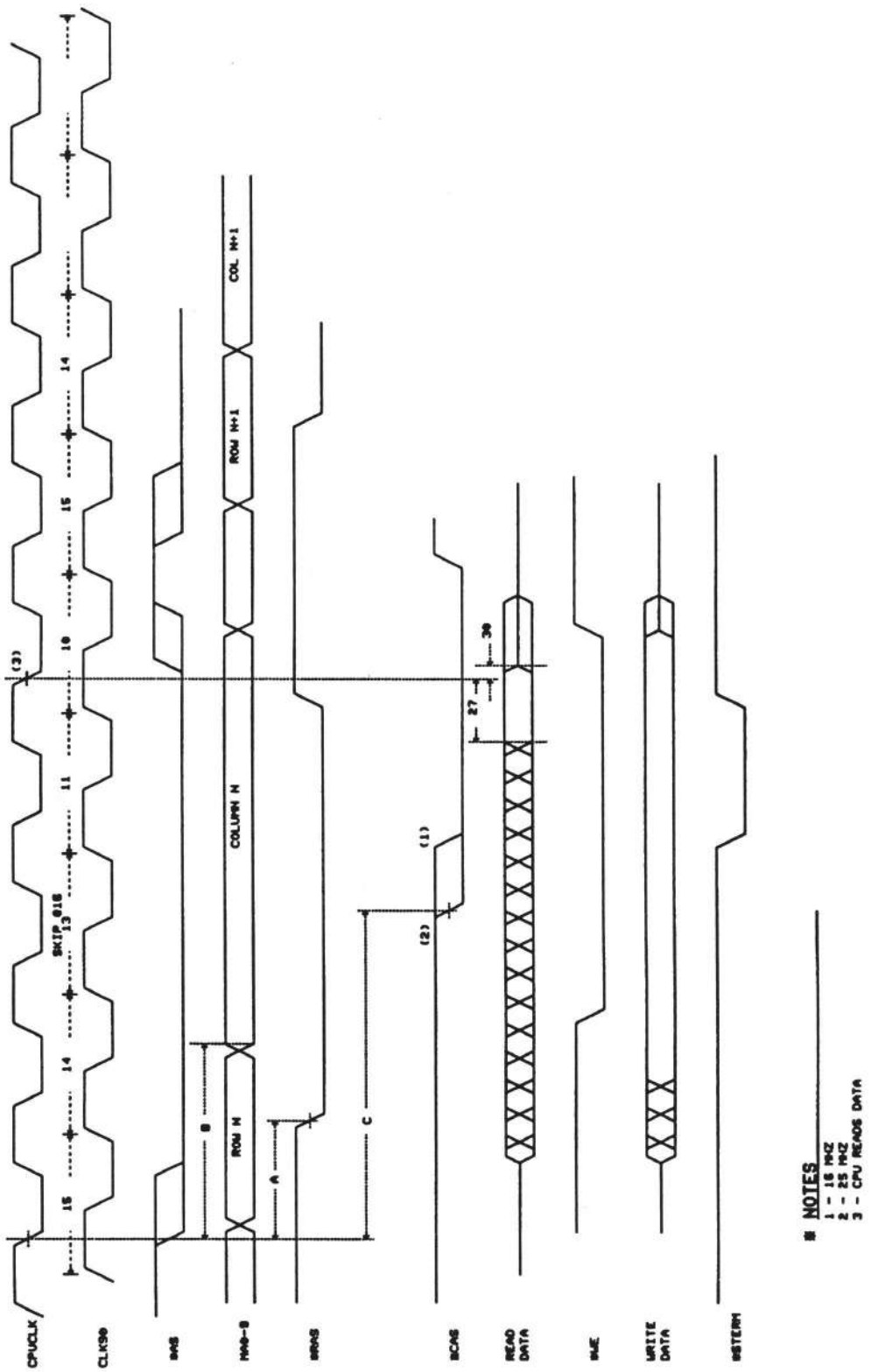


Figure 6-15. Standard RAM Access Timing Diagram (Page Mode Off)

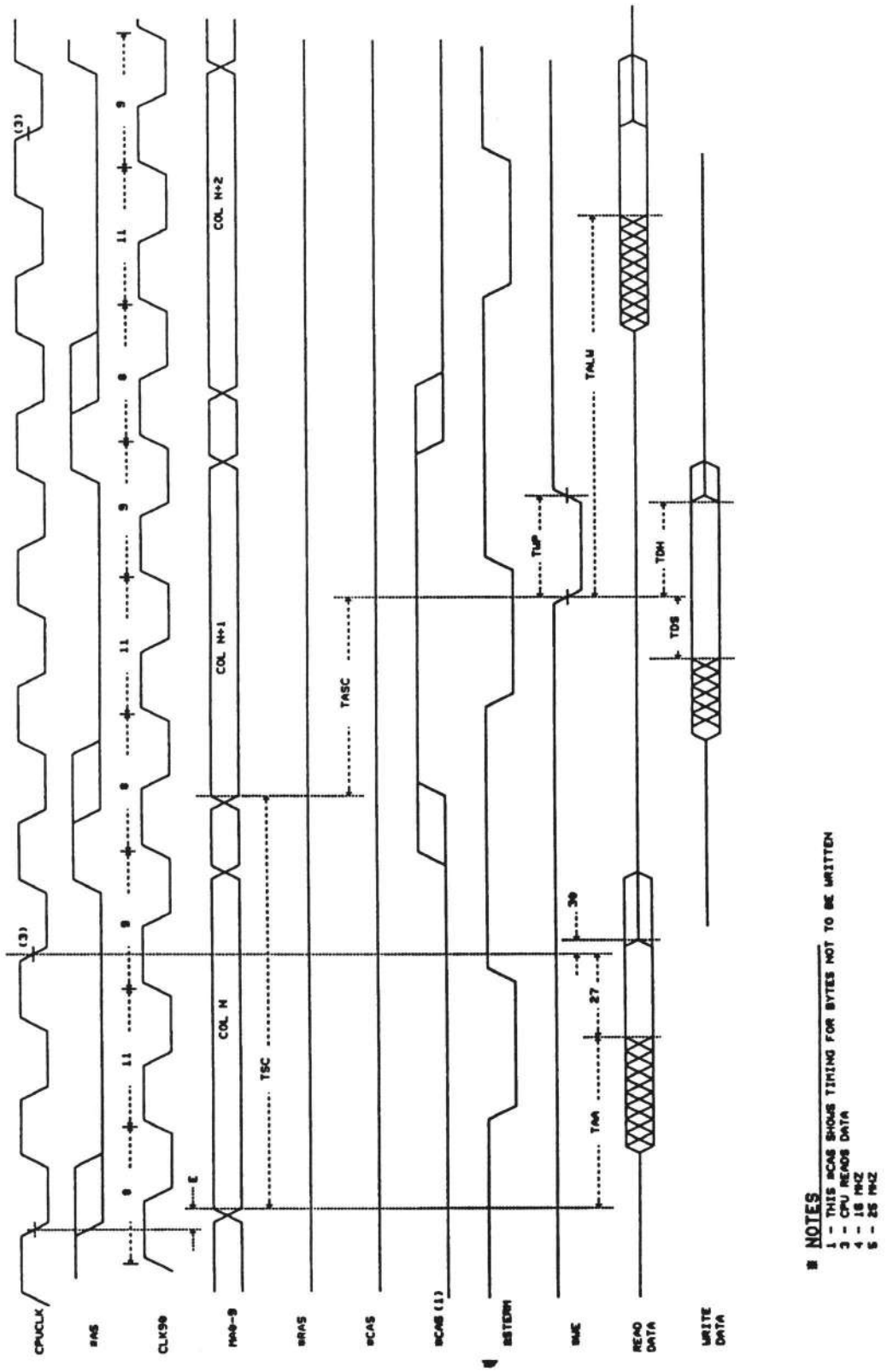


Figure 6-16. RAM Access Timing Diagram (Page Hit, Mixed Read/Write)

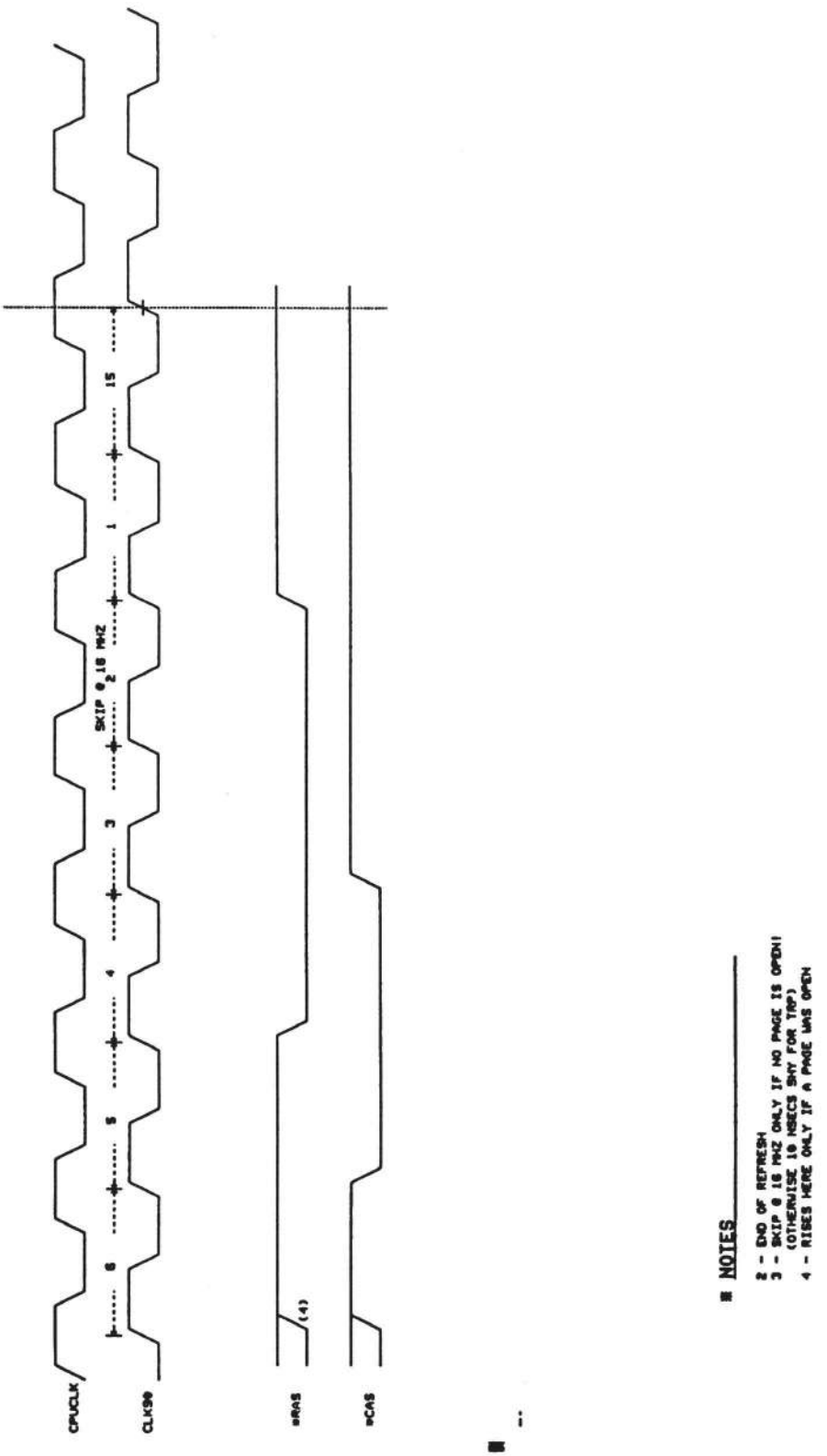


Figure 6-17. Refresh Timing Diagram

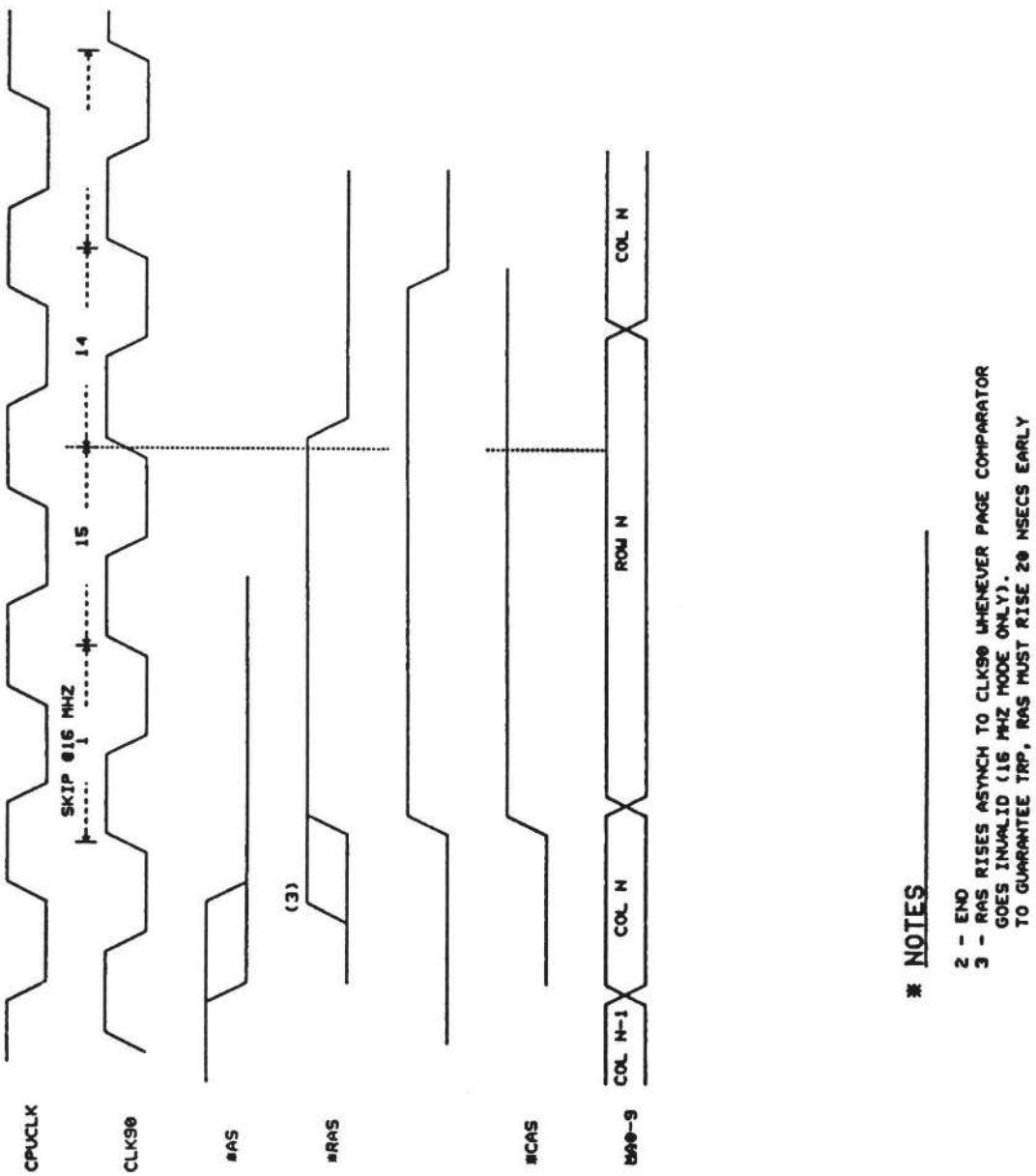


Figure 6-18. Timing Diagram for Closing a Page

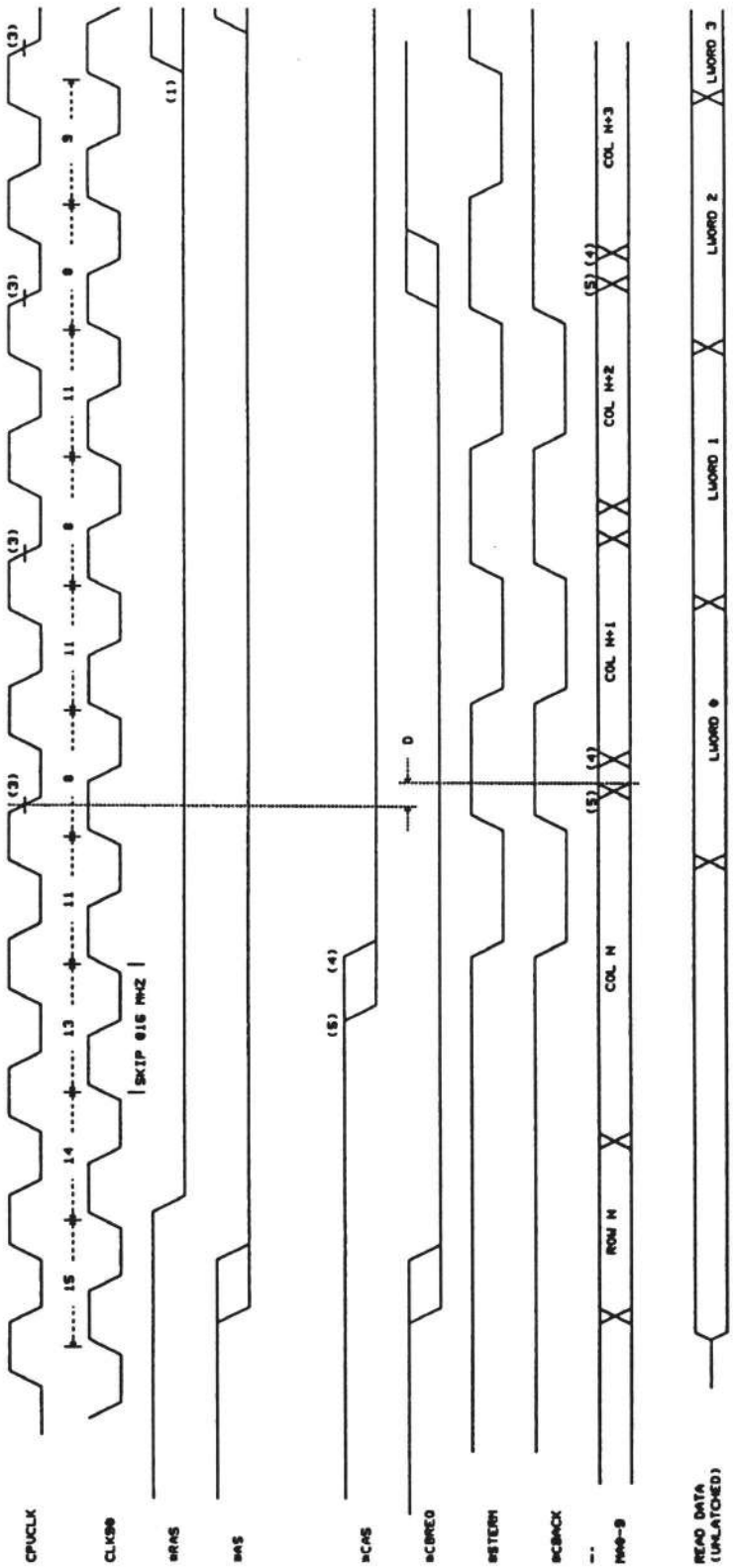


Figure 6-19. Burst Read Timing Diagram (No Page Was Open or Was Just Closed)

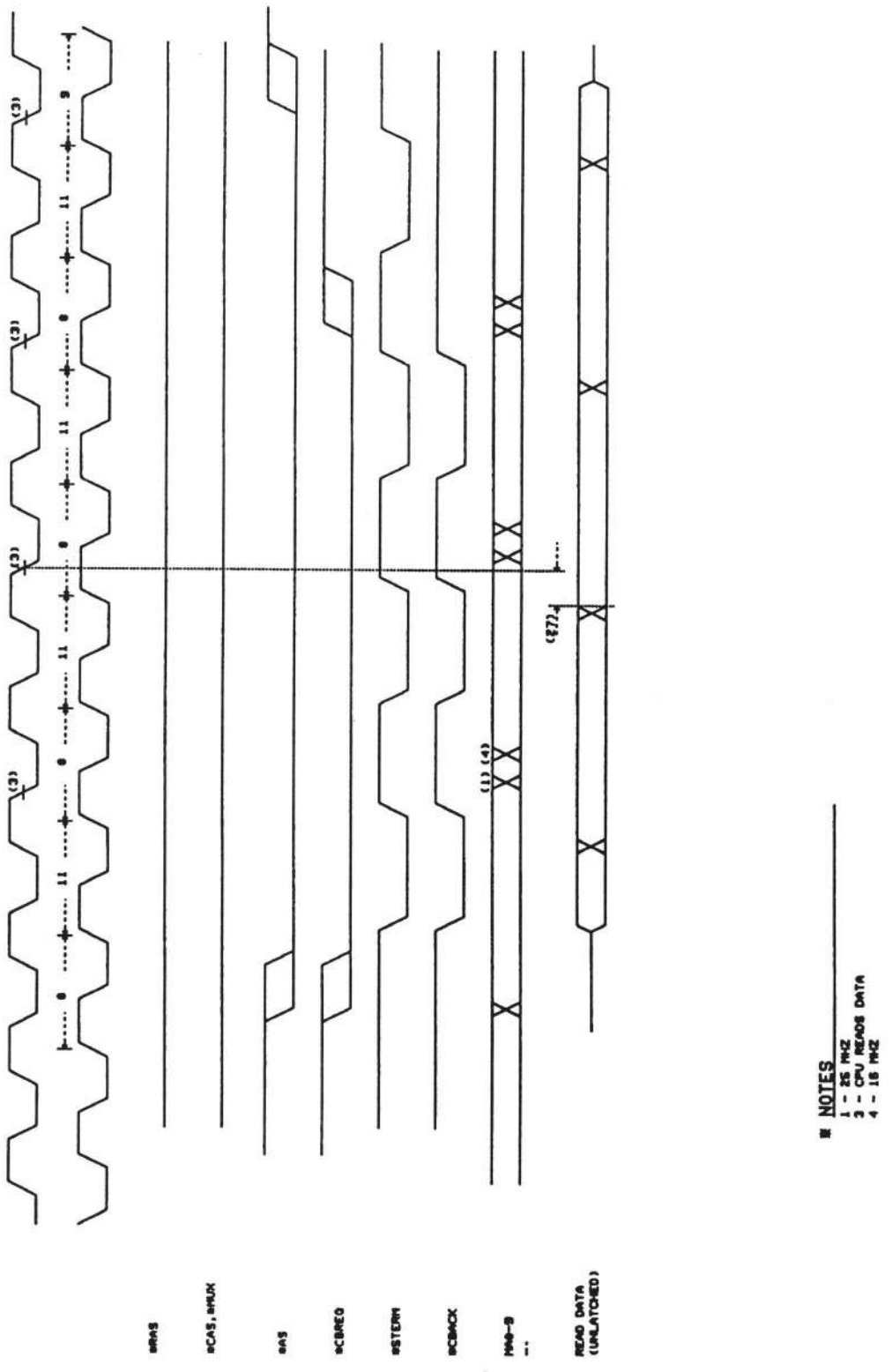


Figure 6-20. Burst Read (Page Hit)

Process Qualification Tests

Integrated circuits supplied to the requirements of this specification shall meet the requirements of Engineering Policy No. 1.02.008. Supporting documentation shall be supplied by vendor upon request.

Environmental Test Conditions

Devices shall comply with the following environmental resistance tests per Commodore Engineering Policy 1.02.007.

1. Temperature/humidity (85° C and 85% RH non-condensing) for 168 hours
2. Operating life (1000 hours at 70° C ambient temperature)
3. Solderability per MIL-STD-883, Method 2003
4. Pressure cooker (15 psig, 120° C, and 100% RH for 24 hours)
5. Solvent resistance per MIL-STD-883, Method 2015, using water and trichloroethane
6. Solder temperature resistance (250° C for five seconds)

Note Devices shall meet this specification's operating performance requirements after the above tests are completed.

Minimum Acceptance Level

The minimum acceptance level of any lot shall be an AQL of 0.65 as defined by MIL-STD 105 single sampling techniques.

Age Of Devices

Unit shall be rejected if EIA Date Code indicates an age of three (3) or more years.

Markings

Devices shall be marked with Commodore part number and copyright notice (© CBM 1989/90) and vendor part number (50012).

BUSTER Chip Specification

Description

This specification describes the requirements for an integrated circuit which is a bus controller gate array.

Configuration

The device shall be configured as a standard 84-pin Plastic Leaded Chip Carrier with external dimensions as shown in Figure 6-21. Refer to Figure 6-22 for connection diagram.

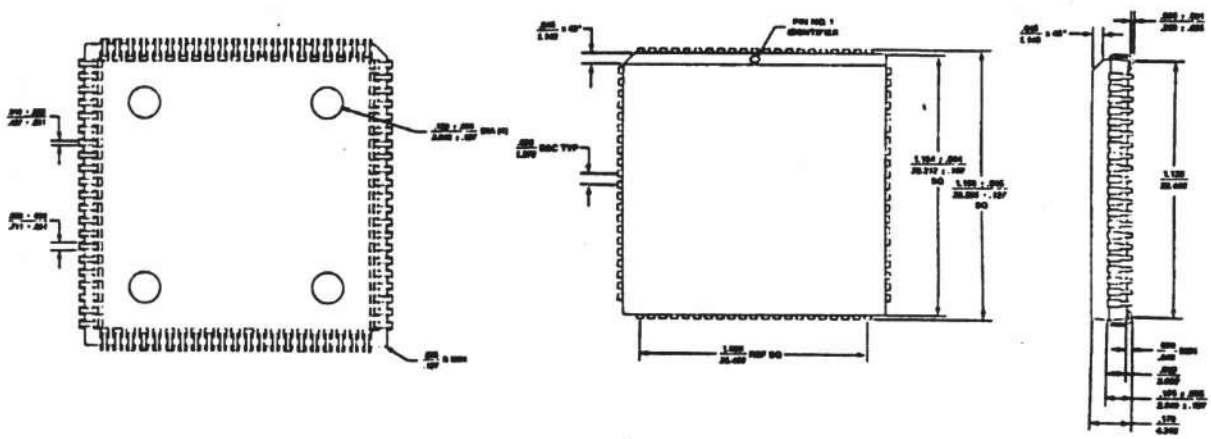


Figure 6-21. External Dimensions

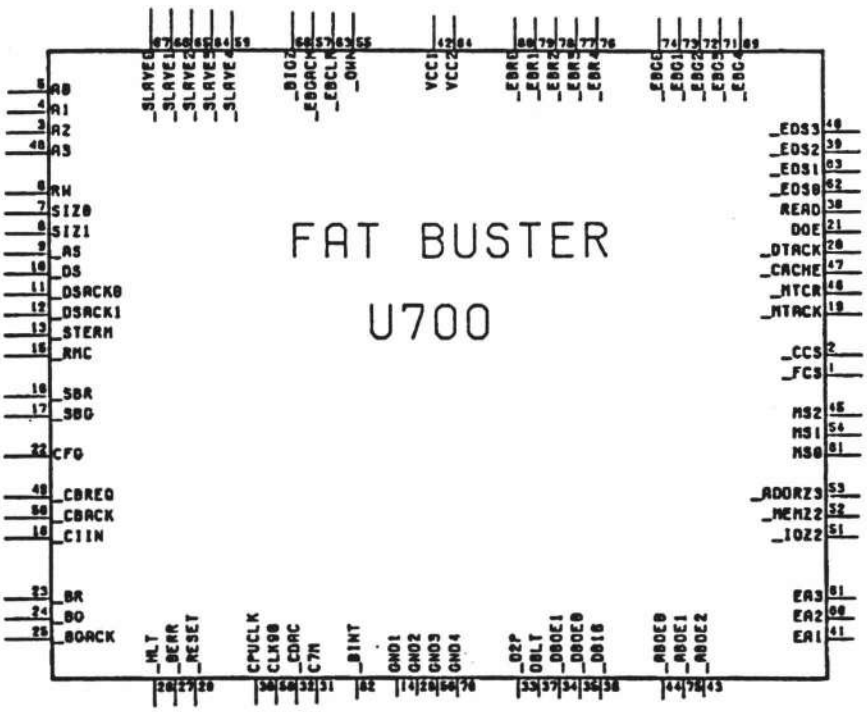


Figure 6-22. Connection Diagram

Sources

Refer to *Approved Vendor List* on page 6-58.

Process Qualification Tests

Integrated circuits supplied to the requirements of this specification shall meet the requirements of Engineering Policy No. 1.02.008. Supporting documentation shall be supplied by vendor upon request.

Environmental Test Conditions

Devices shall comply with the following environmental resistance tests per Commodore Engineering Policy 1.02.007.

1. Temperature/humidity (85° C and 85% RH non-condensing) for 168 hours
2. Operating life (1000 hours at 70° C ambient temperature)
3. Solderability per MIL-STD-883, Method 2003
4. Pressure cooker (15 psig, 120° C, and 100% RH for 24 hours)
5. Solvent resistance per MIL-STD-883, Method 2015, using water and trichloroethane
6. Solder temperature resistance (250° C for five seconds)

Note Devices shall meet this specification's operating performance requirements after the above tests are completed.

Minimum Acceptance Level

The minimum acceptance level of any lot shall be an AQL of 0.65 as defined by MIL-STD 105 single sampling techniques.

Age of Devices

Unit shall be rejected if EIA Date Code indicates an age of three (3) or more years.

Markings

Devices shall be marked with Commodore part number and copyright notice as follows:
© CBM 1989.

FAT GARY Chip Specification

Description

FAT GARY (which will subsequently be referred to as simply 'GARY') is a custom gate array IC used in the A4000. It is packaged in an 84-pin chip, whose pinout is shown below. GARY provides many different 'glue' functions for the system. These functions are:

- Address decoding and timing for ROM
- Address decoding and timing for Chip RAM
- Address decoding and timing for chip registers
- Address decoding and timing for 8520s (CIAs)
- Address decoding and timing for Real Time Clock (RTC)
- Address decoding for the Floating Point Unit (FPU)
- Address decoding for the SCSI/DMA controller IC
- Address decoding for the local bus card slot of the A3000
- Monitoring of the bus for timeout conditions
- Generation of ECLK clock signal
- Generation of 32-bit and 16-bit data strobe signals
- Decoding for generation of AUTOVECTOR (*AVEC) signal to 68030
- Selection of the AGNUS clock source
- System RESET logic
- System INTERRUPT control

Configuration

The device shall be configured as a standard 84-pin Plastic Leaded Chip Carrier with external dimensions as shown in Figure 6-23. Refer to Figure 6-24 for connection diagram.

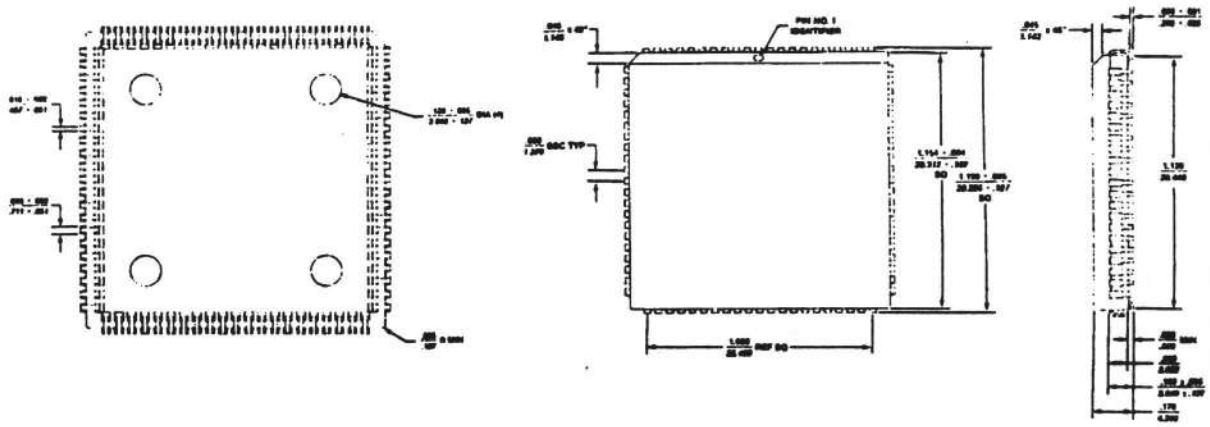


Figure 6-23. External Dimensions

Figure 6-24. Connection Diagram

Sources

Refer to *Approved Vendor List* on page 6-58.

Pin Descriptions

Name	Dir	Description
CPUCLK	Input	
CLK90	Input	CPUCLK shifted 90 degrees.
28M	Input	
7M	Input	
*CDAC	Input	
C1	Input	
C3	Input	
XCLK	Input	
AGCLK	Output	
OVL	Input	Overlay. When high, ROM is mapped in at $00000000 in place of Chip RAM.
ROMJP0,1	Input	ROM jumpers. Used to select ROM access speed.
*AS	Input	68030 address strobe.
*DS	Input	68030 data strobe.
RW	Input	68030 read/write signal.
SIZ0-1	Input	68030 sizing information.
FC0-2	Input	68030 function code bits.
A0,1,12-23	Input	68030 address bits.
A24-31	Bi	68030 address bits.
*BIGZ	Input	When low, address bits A24-31 become outputs, and drive these lines low.
D31	Bi	68030 data bit. Used to communicate with internal registers.
*FPU	Output	Floating Point Unit chip select.
*ROMOE	Output	Output enable signal for the ROM.
*SLOT	Output	Select signal for local bus card slot.
*DMAC	Output	Chip select signal for the DMA controller.
*STERM	Output(OC)	68030 Synchronous Termination signal.
*RTCRD	Output	Real Time Clock read signal.
*RTCWR	Output	Real Time Clock write signal.
LADR	Output	Latch address (external latches for 8520s and RTC).
ECLK	Output	Clock whose frequency is 1/10th that of 7M.
*CIA1,0	Output	Chip select signals for the 2 CIAs (8520s).
*DBR	Input	When high, chip bus is available.
*BLS	Output	Blitter slow down. To AGNUS, requesting access to chip bus.
*RAMEN	Output	Select signal for Chip RAM.
*REGEN	Output	Select signal for chip registers.
LCD	Output	Latch chip data. Controls external latches for chip bus data being read by the 68030.
*OECD	Output	Output enable signal for data being read/written on chip bus.
*xxDS	Output	*UUDS, *UMDS, *LMDS, *LLDS. Data strobe signals for a 32-bit port.
*xDS	Output	*UDS, *LDS. Data strobe signals for a 16-bit port.

Name (cont'd)	Dir (cont'd)	Description (cont'd)
*BERR	Output(OC)	Bus error signal.
*CIIN	Output(OC)	Cache inhibit.
*DSACK0,1	Output(OC)	68030 Data Transfer and Size Acknowledge bits.
*AVEC	Output(OC)	AUTOVECTOR signal.
*IENA	Output	Interrupt enable. This bit is controlled by an internal register.
*RESET	Bi	Reset.
*PWRUP	Input	Power Up. When low, an internal bit is set.
*KBCLK	Input	Keyboard clock.
*TEST	Input	Test. Diagnostic use only.

ROM

The onboard ROMs are selected in the address range from $00F80000 to $00FFFFFF. The ROMs are also selected in the range from $000000000 to $0007FFFF when the overlay input signal (OVL) is true (this allows the RESET instructions to be contained in the ROMs). The ROM shows up in data and program space for both the user and supervisor. ROM caching is enabled.

ROM Timing

The ROM timing circuitry provides for four different speed settings, settable by two jumpers on the motherboard. The *STERM signal is used to terminate the CPU bus cycle during a ROM access.

Table 6-6. ROM Speed Jumper Settings

JP1	JP0	CPU cycles
0	0	5
0	1	6
1	0	7
1	1	8

The minimum output enable (Toe) and access (Tacc) times for the ROMs is determined by the following:

Toe = ((# CPU cycles) - 2) * Tcyc - Tgary

Tacc = ((# CPU cycles) - 1) * Tcyc

where

Tcyc = period of a single 68030 clock

Tgary = delay through GARY (30 ns max)

The timing waveform and state diagram for a ROM access is shown in Figure 6-25.

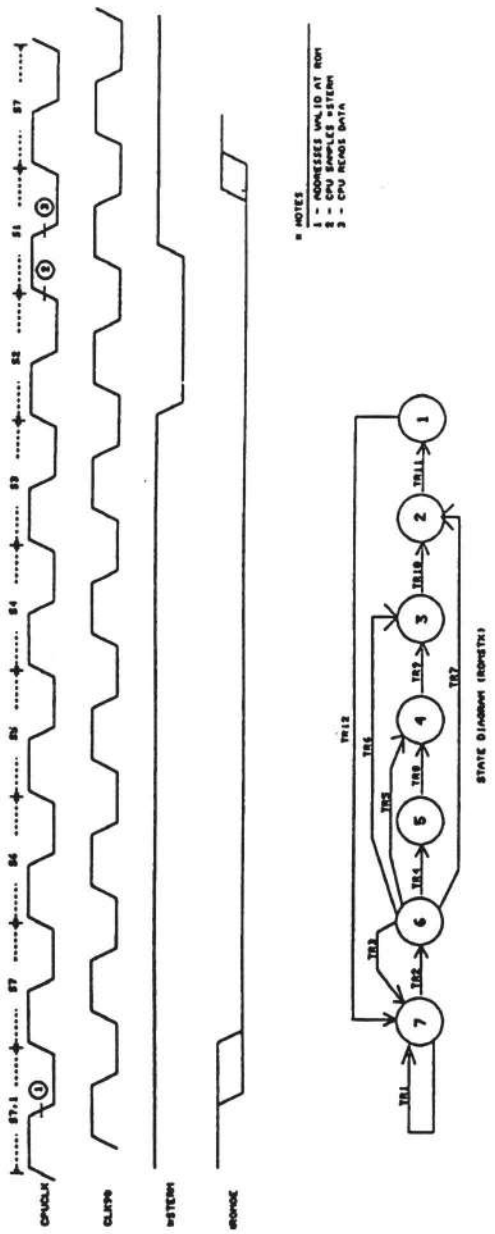


Figure 6-25. ROM Timing

Chip RAM

Chip RAM is selected in the address range from $00000000 to $001FFFFF. When the OVL input is true (high), Chip RAM is not selected for addresses in the range from $00000000 to $0007FFFF (ROM appears here while OVL is true). Chip RAM shows up in data and program space for both the user and supervisor. Chip RAM caching is disabled. The CPU cycle is terminated using both DSACKs, indicating that the Chip RAM data is 32 bits wide.

Chip RAM Timing

Timing for the signals used is shown in Figure 6-26.

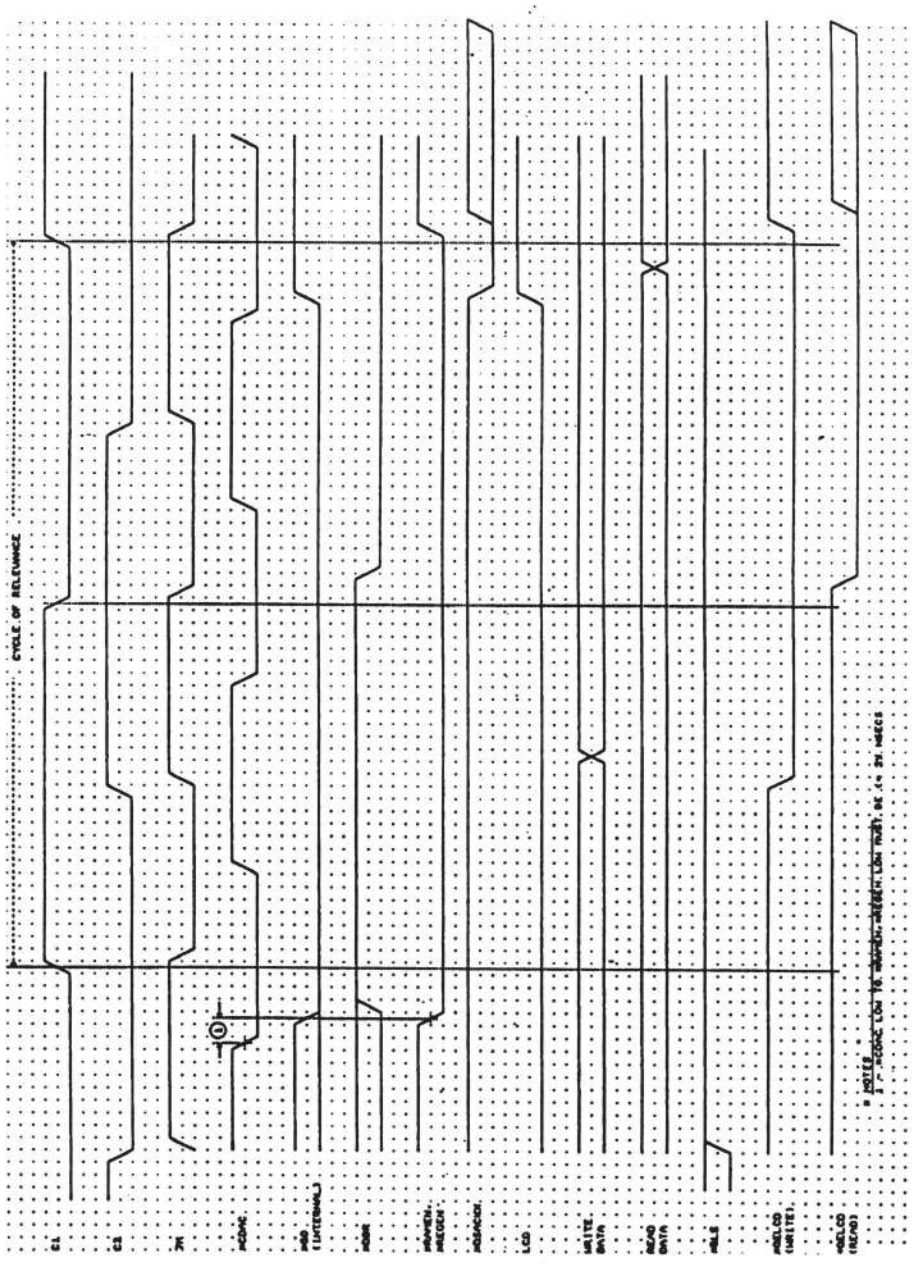


Figure 6-26. CPU Read/Write of Chip Registers and RAM

Chip Registers

The chip registers are selected in the range from $00DFC000 to $00DFFFFF. They also show up from $00C00000 to $00CFFFFF, so that code looking for $C00000 memory will work properly (consequently, C00000 memory is NOT supported). Chip registers show up in user and supervisor data space. Chip register caching is disabled. The CPU cycle is terminated using DSACK1, indicating that the chip registers are 16 bits wide.

8520s

There are two 8520 CIA ICs on the motherboard, referred to here as CIA0 and CIA1. CIA0 is selected in the address range from $00BFE000 to $00BFEFFF. CIA1 is selected from 00BFD000 to 00BFDFFF. The CIAs show up in user and supervisor data space. Caching is disabled. The CPU cycle is terminated by DSACK1, indicating that the CIA is 16 bits wide. In fact, the CIAs are only 8 bits wide, but respond as 16 bits for compatibility. In order to read the 8 bits in on the 68030's D0-D7, CIA0 must be read at an odd word address, and CIA1 must be read at an even word address.

8520 Timing

Figure 6-27 shows the timing for the signals when accessing the 8520s.

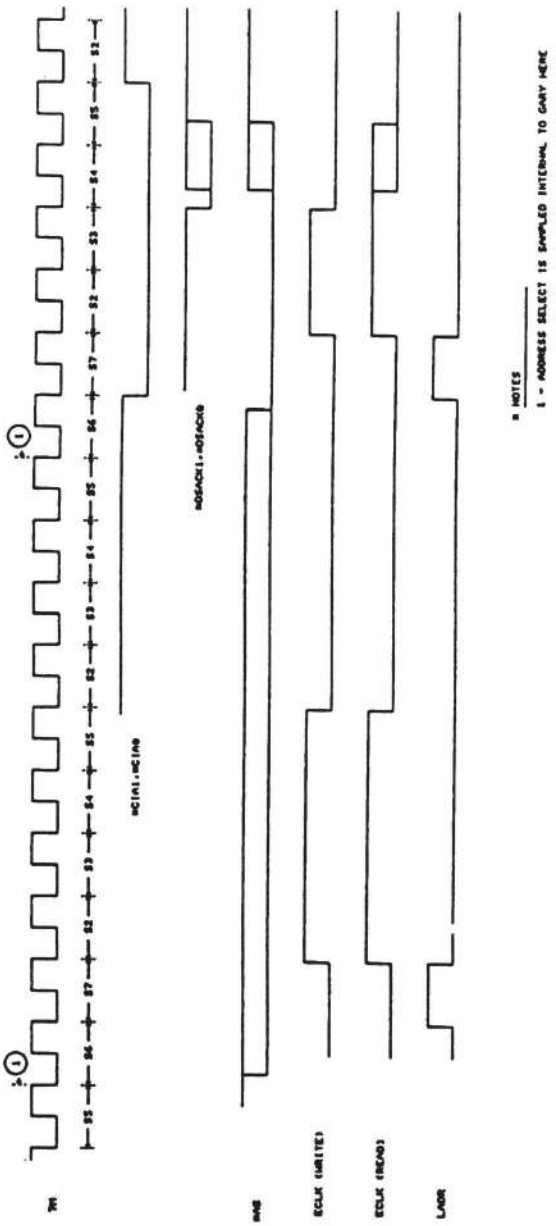


Figure 6-27. 8520 Timing and ECLK Generation

Real Time Clock (RTC)

The RTC is selected in the range from $00DC0000 to $00DCFFFF. It appears in user and supervisor data space. Caching is disabled. The CPU cycle is terminated by DSACK1, indicating that the RTC is 16 bits wide. It is actually only 4 bits, but responds as 16 bits for compatibility. In order to read the 4 bits in on the 68030's D0-D3, the RTC must be read at an odd word address.

RTC Timing

Figure 6-28 shows the timing of the signals for reading and writing to the RTC.

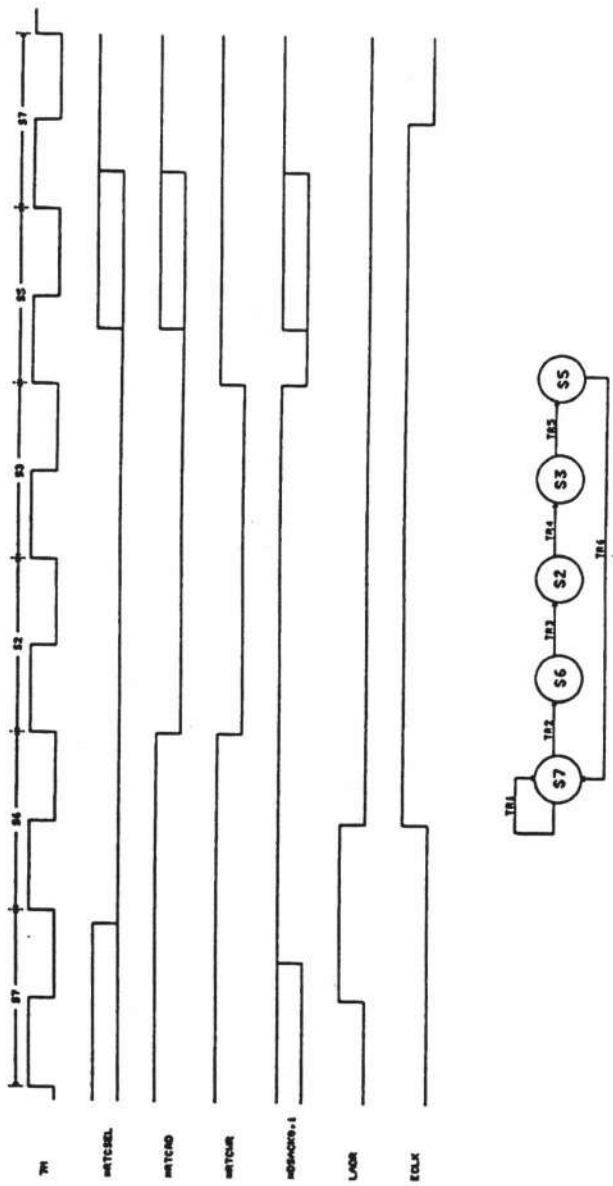


Figure 6-28. Real Time Clock Timing

Floating Point Unit (FPU)

!FPUCS = *AS & FC2 & FC1 & FC0 & !A19 & !A18 & A17 & !A16 & !A15 & !A14 & A13

The FPU performs its own bus cycle termination.

SCSI/DMA Controller

The SCSI/DMA controller is selected from $00DD0000 to $00DD3FFF. It appears in user and supervisor data space. Caching is disabled. In order to get this signal out to the chip as quickly as possible, it is NOT qualified with address strobe (*AS). The SCSI/DMA controller performs its own bus cycle termination.

!DMAC = !FC1 & FC0 & !A31 & !A30 & !A29 & !A28 & !A27 & !A26 & !A25 & !A24, & A23 & A22 & !A21 & A20 & A19 & A18 & !A17 & A16

Local Bus Card Slot

This signal is generated in the address range from $08000000 to $0FFFFFFF. The signal is NOT qualified with *AS. The selection shows up in all address spaces except for CPU space. No bus cycle termination is performed.

!SLOT = FC2 & FC1 & FC0 & !A31 & !A30 & !A29 & !A28 & A27

Bus Timeout

After the assertion of *AS, a counter in GARY starts running, and is reset by the de-assertion of *AS. If the counter counts down before *AS is de-asserted, GARY terminates the cycle automatically. There are two different timer values available, each of which terminates the cycle differently.

There is an 8-bit register in GARY at $00DE0000 of the user and supervisor data space. When written to, bit 7 selects the timeout mode to be used. Writing a 0 to this bit enables DSACK timeout, and a 1 enables BERR timeout (after a RESET, DSACK timeout is enabled). DSACK timeout counts for 32 C1 pulses (approximately 9 μsecs), and then asserts both DSACKs to terminate the cycle. BERR timeout takes much longer, counting for approximately 250 msecs before asserting the *BERR signal. Whenever a bus timeout occurs in either mode, bit 0 of the register at $00DE0000 is set, and is not reset until the register is read.

The purpose of the timeout is to keep the system from getting hung up if an address is asserted that selects nothing. Using BERR mode allows the system to be informed if this occurs.

The DSACK bus timeout mode was made much sorter, and terminates the bus much more 'discreetly' using DSACKs. This mode was made the default because of compatibility issues. The 1.3 ROMs purposely snoop through a large range of address spaces during boot up, which most of the time aren't there. Taking 250 msecs for each one causes it to take forever to boot up. Terminating each bus cycle with *BERR also makes the software get confused. The idea is to get everything running, and then change over to BERR mode.

Since the blitter has the capability of keeping the CPU off of the chip bus for a long time, bus timeout detection is disabled whenever Chip RAM or chip registers are being selected.

Automatic bus timeout can be disabled altogether by writing a 1 to bit 0 of the 8-bit register at $00DE0001. After a RESET, this bit is automatically set to 0 (timeout enabled).

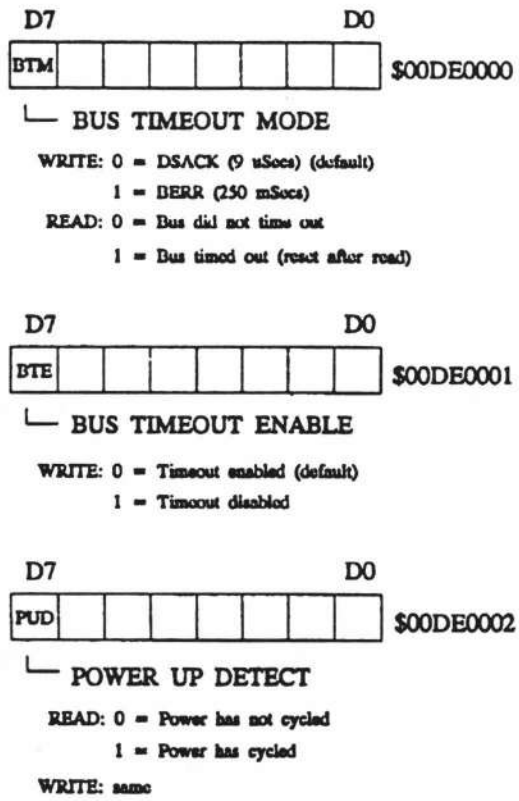


Figure 6-29. Bus Timeout

ECLK Clock

The ECLK signal is generated in GARY. It is a free running clock whose frequency is 1/10th of the 7M clock. Normally ECLK is low for six 7M clocks, and high for four 7M clocks. However, when the CIAs are accessed, the ECLK high time may be shorter than four 7M clocks. During writes to the CIAs, ECLK is high for only two 7M clocks. During reads ECLK stays high for a minimum of two 7M clocks, and a maximum of four 7M clocks. The frequency of ECLK does not change. If the ECLK high time is shortened during CIA access, the difference is made up by increasing the subsequent ECLK low time. Consequently, it is always ten 7M clocks from one rising edge of ECLK to the next.

The ECLK signal is derived from the onboard 28 megahertz oscillator. It is not derived from the XCLK signal when *XCLKE is true. Therefore, ECLK will not change frequency, even when an external system clock source is used (such as when genlocking the video).

Data Strobes

GARY generates six different data strobe signals. Four relate to 32-bit ports (*UUDS, *UMDS, *LMDS, *LLDS), and the other two to 16-bit ports (*DS, *LDS). GARY decodes SIZ1, SIZ0, A1, A0 and RW signals to determine which of the strobes should be active. Whenever RW indicates the CPU is doing a read, all of the strobes are active. Individual strobes are generated during write cycles.

!LDS = !SIZ0 # SIZ1 # A0 # RW

!UDS = !A0 # RW

!UUDS = (!A0 & !A1) # RW

!UMDS = (!A1 & !SIZ0) # (A0 & !A1) # (!A1 & SIZ1) # RW

!LMDS = (!A1 & !SIZ0 & !SIZ1) # (!A1 & SIZ0 & SIZ1) # (A0 & !A1 & !SIZ0) # (!A0 & A1) # RW

!LLDS = (A0 & SIZ0 & SIZ1) # (!SIZ0 & SIZ1) # (A0 & A1) # (A1 & SIZ1) # RW

AUTOVECTOR

When GARY senses that the CPU is doing an exception acknowledge cycle, it generates the AUTOVECTOR signal to tell the CPU to get the exception vectors from RAM.

!AVEC = !AS & FC2 & FC1 & FC0 & A19 & A18 & A17 & A16

AGNUS Clock Source

For genlocking purposes, an external clock can be fed to AGNUS instead of the internal 28 megahertz clock. The clock (XCLK) and the internal 28 meg clock (28M) are both inputs to GARY. The input signal called *XCLKE controls which signal is fed to AGNUS (via the output called AGCLK). When *XCLKE is low, XCLK is output to AGNUS.

!AGCLK = (XCLKE & !28M) # (!XCLKE & !XCLK)

System Reset Logic

GARY controls reset from two different sources. The first is during powerup. The input line called *PWRUP should be kept low via external circuitry until VCC has become stable. The rising edge of *POWERUP causes bit 0 of an 8-bit register at 00DE0002 to be set. The *RESET output is held low for approximately 250 msecs after *PWRUP goes high. This bit can be checked by software to determine what type of reset occurred. The bit can only be reset by writing a 0 back to it (you could just as easily set this bit in order to make the next reset look like a powerup).

The second source of a rest comes from the keyboard. If the input called *KBCLK is held low for at least 60 msecs, the *RESET output will then go low, and will remain low for approximately 250 msecs after *KBCLK goes high again.

System Interrupt Control

Individual system interrupts are controlled by writing to the INTENA register in PAULA. Since this register resides on the chip bus, the CPU is subject to synchronization delays when attempting to access it. Therefore, an alternate method for shutting off ALL of the interrupts in the system is provided in GARY (GARY actually provides only the bit that can be written to — the actual control is done externally in a PAL). The INTENA register in PAULA is located at the offset of $09A. The chip registers occupy only 4K of address space. Consequently, they are 'shadowed' in four 4K chunks from $DFC000 to $DFF000. The 16-bit register in GARY to control interrupts is also located at the offset of $09A, but is selected in the range from $DF8000 to $DFB000 (this register is shadowed at each of the 4K chunks as well). Wiring a 0 to bit 15 of this register will disable ALL of the interrupts going to the CPU. They are re-enabled by writing a 1 to the bit again (the bit is set after a RESET).

Physical Requirements

Marking

Devices shall be marked with Commodore part number plus a copyright notice as follows: © 1989 CBM.

Packaging

The interconnected circuitry shall be contained in a standard 84-pin Plastic Leaded Chip Carrier with external dimensions as shown in Figure 6-23.

Process Qualification Tests

Integrated circuits supplied to the requirements of this specification shall meet the requirements of Engineering Policy No. 1.02.008. Supporting documentation shall be supplied by vendor upon request.

Environmental Test Conditions

Devices shall comply with the following environmental resistance tests per Commodore Engineering Policy 1.02.007.

1. Temperature/humidity (85° C and 85% RH non-condensing) for 168 hours
2. Operating life (1000 hours at 70° C ambient temperature)
3. Solderability per MIL-STD-883, Method 2003
4. Pressure cooker (15 psig, 120° C, and 100% RH for 24 hours)
5. Solvent resistance per MIL-STD-883, Method 2015, using water and trichloroethane
6. Solder temperature resistance (250° C for five seconds)

Note Devices shall meet this specification's operating performance requirements after the above tests are completed.

Minimum Acceptance Level

The minimum acceptance level of any lot shall be an AQL of 0.65 as defined by MIL-STD 105 single sampling techniques.

Age of Devices

Unit shall be rejected if EIA Date Code indicates an age of three (3) or more years.

Approved Vendor List

The following table lists detailed information about the chips described in this document.

This sheet must be removed from this document before the document is shown or transmitted to a vendor.

Commodore Part Number	Description	Vendor	Vendor Part Number
390539-06	FAT BUSTER (sub for 390539-06, 25MHz only)	CSG	4171-013F
390539-07	FAT BUSTER	CSG	4171-013G
390540-01	IC FAT GARY 414 F008A	CSG	4141-008A
390540-02	IC LSI FAT GARY	CSG	4141-008B
390541-04	IC SM CGA FAT RAMSEY PLCC84 RAM Controller	CSG	50012D
390541-07	IC SM CGA FAT RAMSEY PLCC84 A1000+ RAM Controller	CSG	50012G
391380-01	IC Gate Array BRIDGETTE A2200	NCR	BRIDGETTE

Chapter 7

Schematics

A4000 PCB Assembly Schematics

The PCB assembly schematics include the following:

- CPU, FPU clocks, etc.
- FAT GARY, ROM information
- ROMS, RTC, keyboard, power in
- ALICE
- Chip RAM
- Serial port
- Parallel port, floppy
- Audio
- LISA
- Expansion bus connector
- Local bus / coprocessor connector
- BUSTER and expansion bus logic
- Fast RAM
- AT IDE hard disk interface
- Mouse and joystick connectors