COMMODORE AMIGA A1200

Schematics

rev 1 www.amigawiki.org

Revision History

REV	DESCRIPTION	DATE	APRVL	MANAGER
0	Engineering Prototype	03/13/92	GRR	
1	Advance Engineering Release	06/29/92	GRR	
1a	Pilot Production Release	09/09/92	GRR	
1b	FTZ Production Release	09/09/92	GRR	
1d	FCC/FTZ Production Release	10/10/92	GRR	

Jumpers and Stuff

REF	TYPE	DESCRIPTION	PAGE
R246	SMT	NTSC Color Burst	4
R202	SMT	PAL Color Burst	4
R625	SMT	Keyboard MPU Clock	9
R624	SMT	Keyboard/System Reset	9

Connectors

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	Mouse/Joystick 1	5
CN2	DB9P	Mouse/Joystick 2	5
CN3	RCA-J	Right Audio Output	5
CN4	RCA-J	Left Audio Output	5
CN5	DB23S	External Floppy	8
CN6	DB25P	RS232 Serial Port	7
CN7	DB25S	Parallel Printer Port	7
CN8	SQ DIN	Power Supply Connector	13
CN9	DB23P	Video Output	6
CN10	RCA-J	Composite Video	4
CN11	DIL-34	Internal Floppy Signal	8
CN12	SIL-4	Internal Floppy Power	8
CN13	MEM-30	Keyboard Membrane	9
CN14	SIL-4	Internal Floppy Power	8
CN13	MEM-30	Keyboard Membrane	9
CN14	SIL-4	Keyboard Status LED's	9
CN15	PCMCIA	PC"Memory Card"	11
P9	EDGE-80	Memory Bus Expansion	12

Signal Glossary

SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHz Master Clock	
7MHZ	7.15909 MHz Processor Clock	
A[23:1]	Processor Address Bus (68000)	
ACK	Data Acknowledge (Parallel Port)	
AS	Address Strobe (68000)	
AUDIN	Audio Input (RS232 Port)	
AUDOUT	Audio Output (RS232 Jack)	
BEER	Bus Error (68000)	
BG	Bus Grant (68000)	
BGACK	Bus Grant Acknowledge (68000)	
BLISS	Blitter Slowdown (Chips)	
BLIT	Chip Memory Access (Chips)	
BR	Bus Request (68000)	
BUSY	Device Busy (Parallel Port)	
CASL/U	Column Address Strobe (DRAM)	
CCK/CCKQ	Color Clock / Quadrature (Chips)	
CDAC	7.15909 MHz Quadrature Clock (Chips)	
CHNG	Media Change (Floppy)	
CLKRD/WR	Read-Time Clock Read / Write (RTC)	
COMP	Monochrome Composite Video (Video)	
CSYNC	Composite Sync (Video)	
CTS	Clear to Send (RS232 Port)	
D[15:0]	Processor Data Bus (68000)	
DIR	Step Direction (Floppy)	
DKRD	Disk Read Data (Floppy)	
DKWD	Disk Write Data (Floppy)	
DKWE	Disk Write Enable (Floppy)	
DMAL	Chip DMA Request Line (Chips)	
DRA[8:0]	DRAM Address Bus (DRAM)	
DRD[15:0]	DRAM Data Bus (DRAM)	
DSR	Data Set Ready (RS232 Port)	
DTACK	Data Transfer Acknowledge (68000)	
DTR	Data Terminal Ready (RS232 Port)	
E	Peripheral Enable Clock (68000)	
EXTICK	Expansion Present / RTC Tick	
FC[2:0]	Function Code (68000)	
FIRE0/1	Fire Button 0/1 (Joysticks)	
HLT	Processor Halt (68000)	
HSYNC	Horizontal Sync (Video)	
INDEX	Index Pulse (Floppy)	
INT[2,3,6]	Interrupt Request (Chips)	
IORESET	I/O Reset	
IPL[2:0]	Interrupt Priority Level (68000)	
KBCLOCK	Keyboard Clock (Keyboard)	
KBDATA	Keyboard Data (Keyboard)	
KBRESET	Keyboard Reset (Keyboard)	
LDS/UDS	Upper / Lower Data Strobes (68000)	
LED	Power On LED / Audio Filter Disable	
LEFT/RIGHT	Left Right Audio (Audio)	

SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	Light Pen Trigger (Joysticks)	
MTR	Motor On (Floppy)	
MTR0	Motor On - Drive 0 (Floppy)	
M0V/M0H	Mouse 0 Quadrature V/H (Joysticks)	
M1V/M1H	Mouse 1 Quadrature V/H (Joysticks)	
OVL	Overlay ROM over RAM	
OVR	Override System Decoding	
PIXELSW	Genlock Pixel Switch (Video)	
POT0X/0Y	Pot Lines 0 X/Y (Joysticks)	
POT1X/1Y	Pot Lines 1 X/Y (Joysticks)	
POUT	Paper Out (Parallel Port)	
PPD[7:0]	Parallel Port Data (Parallel Port)	
RAMEN	RAM Enable (Chips)	
REGEN	Chip Register Enable (Chips)	
RAS0/1	Row Address Strobe (DRAM)	
RDY	Drive Ready (Floppy)	
RESET	General Reset	
RGA[8:1]	Register Address Bus (Chips)	
R/G/B	Red / Green / Blue (Video)	
RI	Ring Indicate (RS232 Port)	
ROMEN	ROM Enable (ROM)	
RTS	Request to Send (RS232 Port)	
RST	Processor Reset (68000)	
RXD	Receive Data (RS232 Port)	
RW	Processor Read/Write (68000)	
SEL	Select (Parallel Port)	
SEL[3:0]	Drive Select (Floppy)	
SIDE	Side Select (Floppy)	
STEP	Step In/Out Command (Floppy)	
TRK0	Track Zero Sense (Floppy)	
TXD	Transmit Data (RS232 Port)	
VMA	Valid Memory Address (68000)	
VPA	Valid Peripheral Address (68000)	
VSYNC	Vertical Sync (Video)	
WE	Write Enable (DRAM)	
WPROT	Write Protect Sense (Floppy)	
XCLK	External Genlock Clock (Video)	
XCLKEN	External Clock Enable (Video)	
XRDY	External Data Ready	
	** Credit Card and IDE Stuff? **	

Key Components

REF	CHIP	DESCRIPTION	PAGE
U1	68000	68000 Processor 16MHz	2
U2	8374	Alice (AA Agnus)	2
U3	8364	Paula	5
U4	4203	Lisa (AA Denise)	4
U5	f023a	AA Gayle (CBM ASIC)	2,8,11
U6	asst	ROM 512Kx16, 150 nS	10
U7-8	8520	Amiga VIA, 1 MHz	7
U10-11	28F10	Flash Memory 128Kx8	10
U12	CXA1145	Sony Video Encoder	4
U13	68HC05	amiga Keyboard MPU	9
U49	PST518	Low Voltage Sense IC	9
U15	LF347	BiMOS Op-Amp	5
	TL084	BiCMOS Op-Amp	alt
U16-17	Asst	DRAM 256Kx16, 80nS	3
U18-19	Asst	DRAM 256Kx16 Optional	3
U20	391???	Budgie (ASIC)	2
U28	1488	EIA Line Driver	7
U29	1489	EIA Line Receiver	7
U30	BT101	Triple 8-bit Video DAC	4
X1	OSC	TTL 28.63636 MHz NTSC	2
	OSC	TTL 28.37512 MHz PAL	alt
Y451	XTAL	4.43619MHz PAL Burst	4
Y621	XTAL	3MHz Ceramic Resonator	9
X2	asst	PAL Video Modulator	4
	asst	NTSC Video Modulator	4

A1200 Rev 1->1d PCB

DIRECTORIES AND REVISION HISTORY

C.A.D. Generated
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DESIGN BY: G. Nakano 09/15/92
DRAW. CHK 10/16/92
ENGR. CHK 09/09/92
CHKD.
APPR.
USED ON: C/A1200
NEXT ASSY: 364718

Commodore
Schematic A1200 R1d
C/A1200 Main Board
"Channel Z"
SIZE C 364717 REV 1a
SCALE
SHEET 1 OF 13
PATH: /project/a300/channel_z.cvi sheet1

Channel Z
10/10/92

OOPS!

All this stuff serves to correct one minor Gayle bug and a number of Alice deficiencies not yet corrected.

Assuming the changes are implemented in the production Gaule chip, then all this sillyness is best erased...

Reference	Old Gayle	New Gayle
XU1	74F74	none
XU2	74F02	none
XU3	74F74	none
U26X	74F86	none
XJ4	0 Ohm	out
XJ1	out	0 Ohm
XJ2	out	0 Ohm
XJ3	out	0 Ohm
U26	note	74LS86

U1 MC68EC020

U0 MC68881

U2 8374 ALICE

U20 BUDGIE 391425 CLOCK PART

U5 4145f023a AA_GAYLE

XU9

OOPS! - 32-bit / slow ROM
XJ9 in - add ROM wait

Note: PAL uses 28.37516 MHz

Note: Various components are for EMI Control and may be loaded with funny things...

CONTROL FUNCTIONS

PROCESSOR AND OTHER USEFUL COMPONENTS

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DESIGN BY:	S. Rumkins
Drawn:	GMR
CHK'D:	
APPD:	
USED ON	C/A1200
NEXT ASSY	364718
SIZE	C
DRAWING	364717
REV	1a
SCALE	
SHEET	2 OF 13

Commodore
Schematic A1200 Rid
C/A1200 Main Board
"Channel Z"

PATH: /project/a300/channel_z.rev1 sheet2

A1200 Rev 1->1d PCB

DRD(31:0)

DRA(9:0)

BDRA(8:0)

D(31:0)

U20

391425
BUDGIE

BRIDGE/DRAM PART

U16

U17

DRAM

256Kx16

U18-19 Optional

U18

OPT

U19

OPT

_RAS
_CAS
_DWE
_DBR
A(1)
A(0)
SIZE_1
SIZE_0
R_W
_DS
_OEB
_RST

_ROE
_BRAS(1)
_BRAS(0)
_BCAS_UU
_BCAS_UM
_BCAS_LM
_BCAS_LL
_BWE
_BCAS_XX
_UDS
_LDS

R151A R151B R151C R151D R151E R151F R151G R151H R151I

R152A R152B R152C R152D R152E R152F R152G R162 R163 R164

C152A C152B C152C C152D C152E C152F 22pF

R161 470

VCC

C16A C16B C17A C17B C18A C18B C19A C19B 0.22uF

U16 U17 OPT U18 OPT U19 OPT

DECOUPLING

DECOUPLING

A1200 Rev 1->1d PCB

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MEMORY AND...WELL, I USED TO REMEMBER

DESIGN BY: C. Rohlin	DATE: 01/15/91	Commodore
DRAW: GMR	4/17/91	
CHKD: GMR	05/09/91	Schematic A1200 R1d
APPD:		C/A1200 Main Board
USED ON: C/A1200	NEXT ASSY: 315738	"Channel Z"
SIZE: C	364717	REV: 1a
SCALE	SHEET 3 OF 13	

PATH: /project/a500/channel_z.rev1 sheet3

A1200 Rev 1->1d PCB

U4 LISA 4203

U30 BT101 VIDEO DAC

VIDEO DAC

U32 74HCT244

U23 74F139

U12 CXA1145 ENCODER

COMPOSITE

COLOR

CN10

MODULATOR

X2

PAL ONLY

M/N-PAL OPTION
ADDED REV 1E PCB

R209 ADDED REV 1B PCB

DENISE IS PRETTY MUCH INTO VIDEO...

Note: Components designated as Exxx may be loaded with EMI fliters, ferrite beads or resistors!

Commodore
Schematic A1200 R1d
C/A1200 Main Board
"Channel Z"
364717 REV 1a
SHEET 4 OF 13

MOUSE/JOYSTICK PORTS

LEFT JOY
CN1
DB9P CN1A

RIGHT JOY
CN2
DB9P

U34
74LS166

R370
4.7K

U3
PAULA
8364

U15
LF347 /TL084

U28

Q331 MPF102
Q321 MPF102
Q341 2N3906

CN3
RIGHT
RCA JACK

CN4
LEFT
RCA JACK

MDAT
_MLD
CCK_A
_RESET
MONO
AUDOUT
LEFT
RIGHT

Note: LED off, Filters bypassed

AUDIO FILTERS

PAULA PREFERS THE TRADITIONAL MODES

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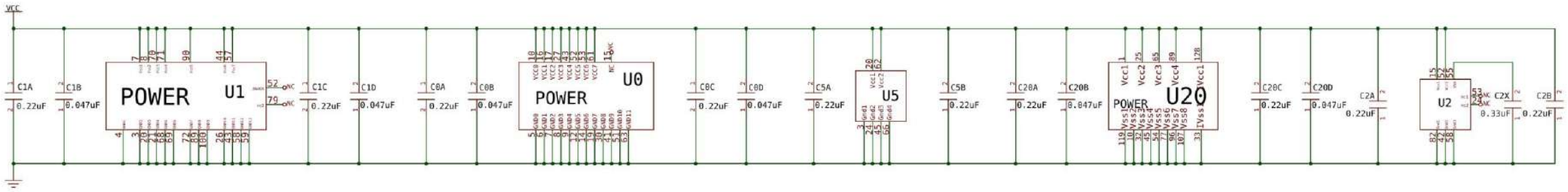
DESIGN BY: C. Rubbins	DATE 05/15/91
DRAW: GDR	10/22/90
LAST: CRR	09/09/91
CHKD:	
APPD:	
USED ON C/A1200	NEXT ASSY 364718

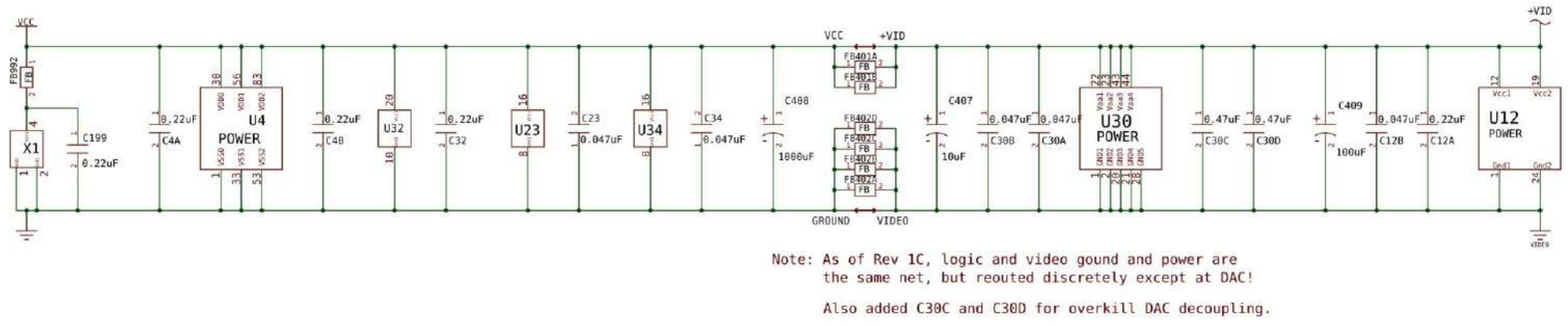
Commodore
Schematic A1200 R1d
C/A1200 Main Board
"Channel Z"
SIZE C 364717 REV 1a
SCALE
SHEET 5 OF 13
PATH: /project/a300/channel_z.rev1 sheet5

A1200 Rev 1->1d PCB

GENERAL DECOUPLING



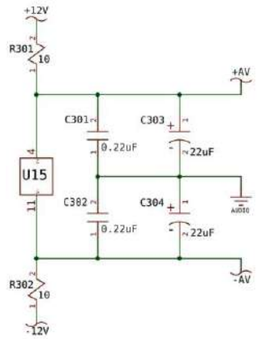
VIDEO DECOUPLING



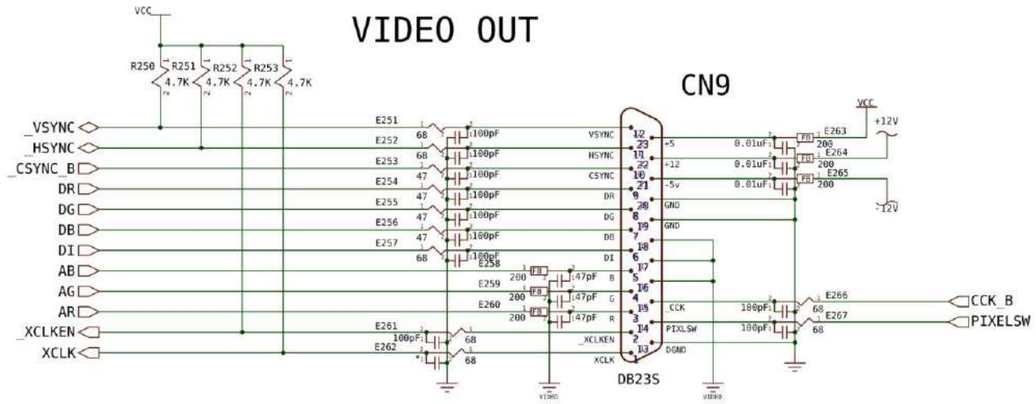
Note: As of Rev 1C, logic and video gound and power are
the same net, but reouted discretely except at DAC!

Also added C30C and C30D for overkill DAC decoupling.

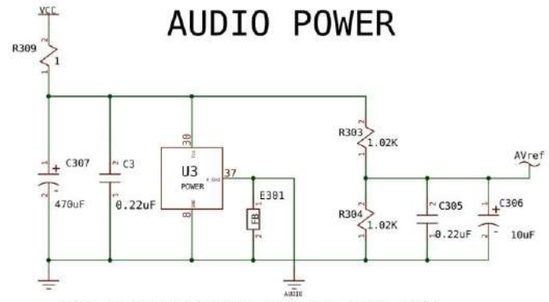
AUDIO DECOUPLING



VIDEO OUT



AUDIO POWER



Note: Ground interconnection near audio jacks.

A1200 Rev 1->1d PCB

PARTY OUT OF BOUNDS, WHAT A MESS...

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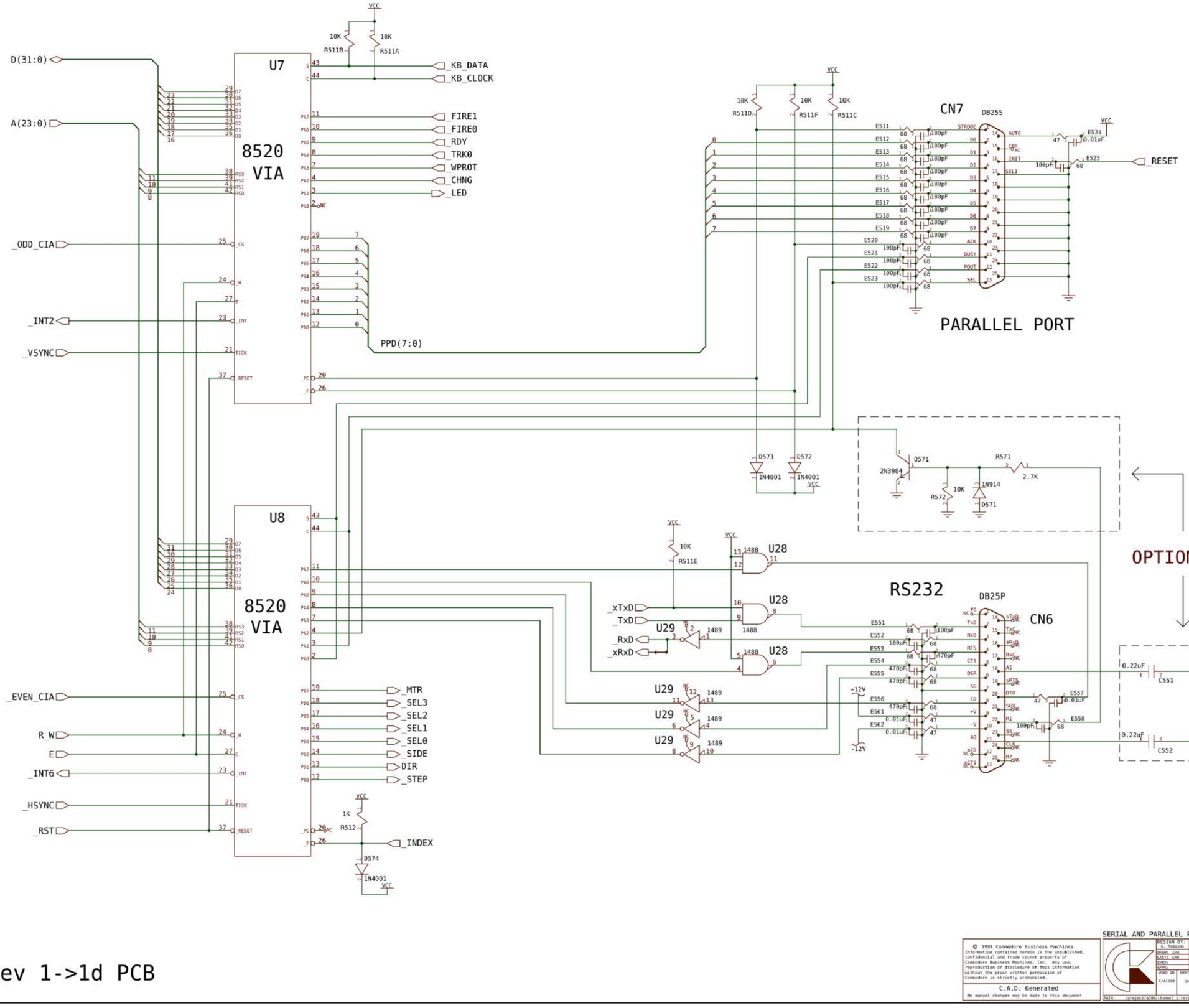
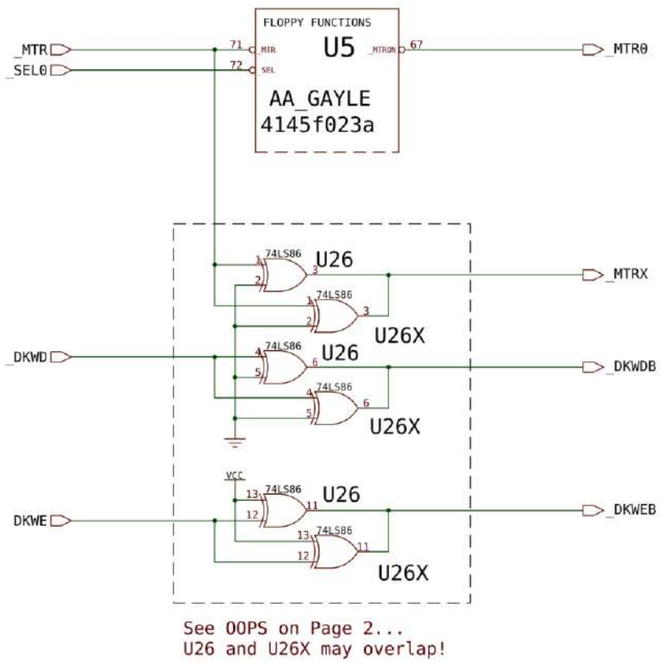
DESIGN BY: C. Robbins	DATE 03/15/92	Commodore
DRAWN: CRB	03/15/92	Schematic A1200 R1d
CHKD:		C/A1200 Main Board
APPR:		"Channel Z"
USED ON C/A1200	NEXT ASSY 364718	SIZE C 364717 REV 1a
		SCALE SHEET 6 OF 13

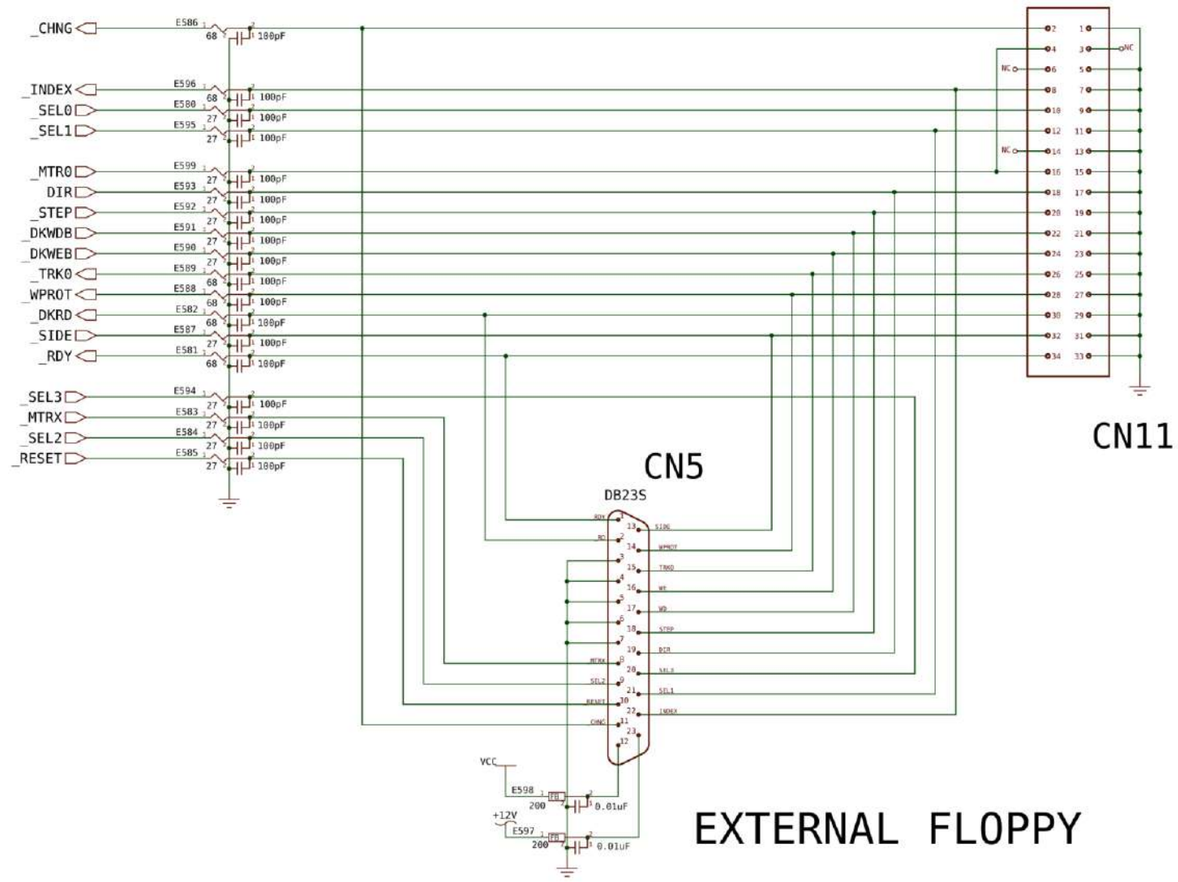
PATH: /project/a1200/channelz/.text sheet6



FLOPPY LOGIC

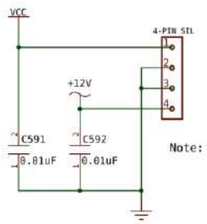


INTERNAL FLOPPY



EXTERNAL FLOPPY

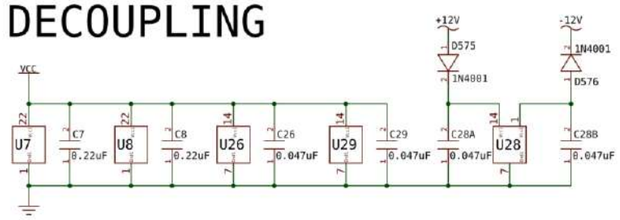
FLOPPY POWER



CN12

Note: Some drives are +5 only...

DECOUPLING



THE REST OF THE FLOPPY STUFF

DESIGN BY	C. Robbins	DATE 01/15/92
DRAW. DEP.		01/15/92
CHK'D.		
APPR.		
USED ON	NEXT ASSY	
C/A1200	364738	

Commodore

Schematic A1200 R1d
C/A1200 Main Board
"Channel Z"

SIZE C | 364717 | REV 1a

SCALE | SHEET 8 OF 13

path: /project/a1200/channel_z.rev1_sheet8

A1200 Rev 1->1d PCB

KEYBOARD TAIL

CN13

MEMBRANE-31

KEYBOARD MPU

U13

68HC05C

KEYBOARD
MICRO

22pF C621 Y621 3MHz R628 1M 22pF C622

OSC2 OSC1

NC1 NC2 NC3 NC4

VCC R621 4.7Kx9

R622 100

R624 4.7Kx9

PD7 PD5 PD4 PD3 PD2 PD1 PD0

PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0

PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0

PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0

TCMP TCAP

IRQ RESET

KB_CLOCK
KB_DATA
KB_RESET
PWR_BAD

R625

R626 *

R623 10K

CN17

7-PIN SIL

KB TEST

NEW ON REV 1E PCB

R629 10K

C629 0.33uF

U49 RH5VA43A

POWER OK

KB LEDS

_IDE_LED R631 10K R632 4.7K Q631 2N3906

_CC_ENA R637 R638 Q634 2N3906

OPTIONAL

_MTR0 R633 10K R634 4.7K Q632 2N3906

_LED R635 10K R636 4.7K Q633 2N3906 R639 100

5-PIN SIL

CN14

U13 POWER C13 0.22uF

A1200 Rev 1->1d PCB

THE NEW HOME OF THE KEYBOARD VIRUS

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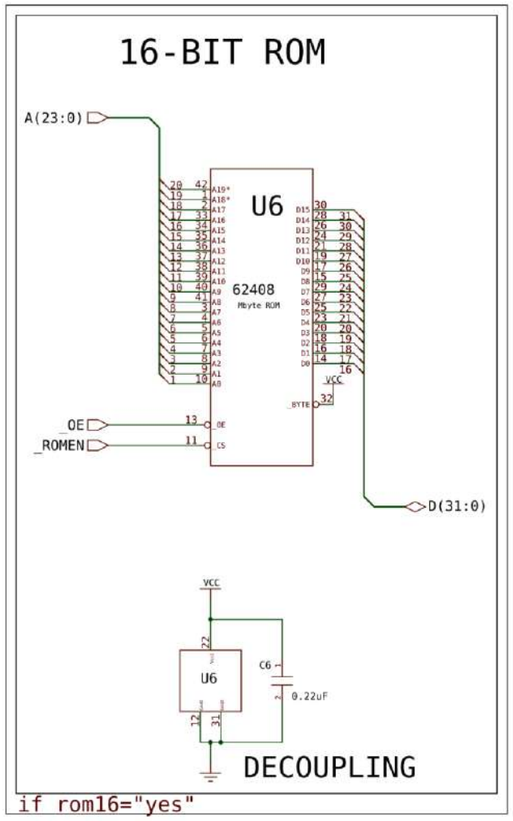
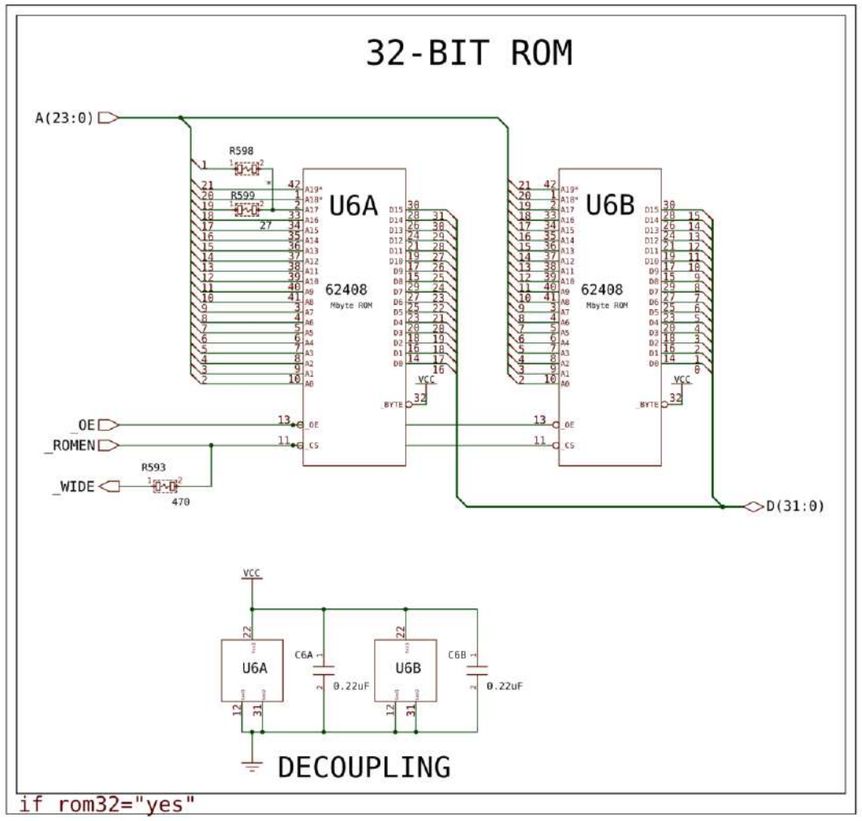
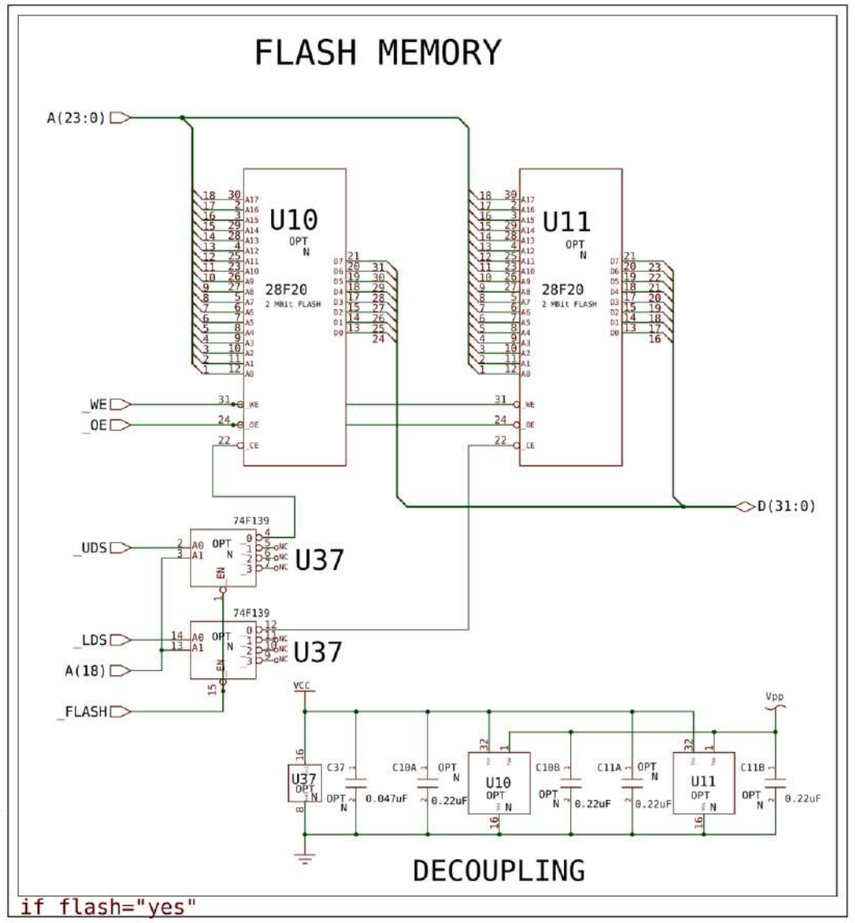
DESIGN BY: C. Robbins	DATE 01/15/92	Commodore
DRAW: CRB	01/15/92	Schematic A1200 R1d
LAST: CRB	09/09/92	C/A1200 Main Board
CHK:		"Channel Z"
APPR:		
USED ON C/A1200	NEXT ASSY 364718	SIZE C 364717 REV 1a
		SCALE SHEET 9 OF 13

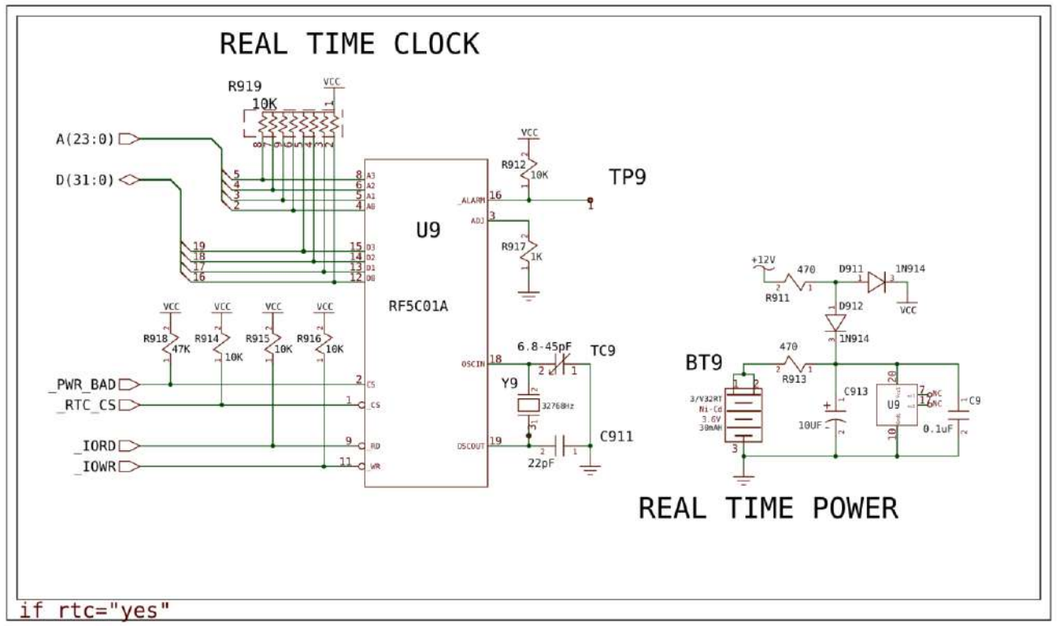
PATH: /project/a500/channel_z.sch1 sheet9





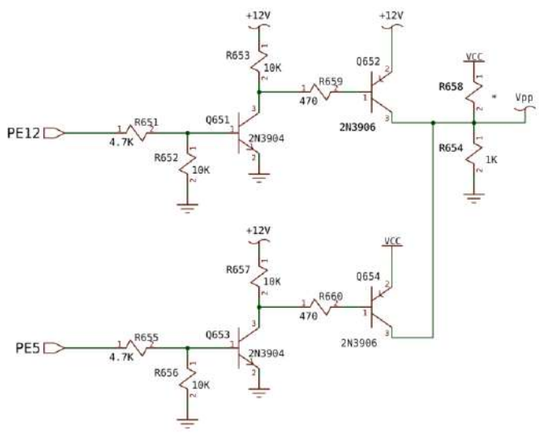


16 AND 32-BIT SOCKETS MAY OVERLAP!



OPTIONAL REAL-TIME CLOCK/CALENDAR

OPTIONAL FLASH MEMORY



A1200 Rev 1->1d PCB

ROM - PLAIN AND FANCY - DODADS TOO!

DESIGN BY	C. Robbins	DATE 03/15/91
DRAW: DBR		03/15/91
CHK'D:		
APPR:		
USED ON	C/A1200	NEXT ASSY 364718

Commodore
Schematic A1200 R1d
C/A1200 Main Board
"Channel Z"
SIZE C | 364717 | REV 1a
SCALE
SHEET 10 OF 13
PATH: /project/a1200/channel_z.rev1 sheet10

MEMORY CARD

CN15

A(23:1)

CC_A0

Warning:
Byte Swapped

BUS PART
U20
BUDGIE
391425

U45 74LS245

U46 74LS245

U47 74LS245

R714A 120

R714B 120

CC_D(15:0)

CC_A(25:0)

R701 10K

R716 10K

74LS245
U43

_OE
_WE
_IORD
_IOWR
_UDS
_LDS
_REG
_CC_WAIT

_CC_OE
_CC_WE_PGM
_CC_IORD
_CC_IOWR
_CC_CEU
_CC_CEL
_CC_REG
_WAIT

_CC_ENA

R717 10K

R718 10K

C701 0.22uF

C702 0.22uF

_CC_CD(1)
_CC_CEU
_CC_CEL
_CC_OE
_CC_IORD
_CC_IOWR
_CC_WE_PGM
_CC_BUSY_IREQ
_CC_RESET
_CC_WAIT
_CC_REG
_CC_BVD(2)
_CC_BVD(1)
_CC_WP
_CC_CD(2)

R715 10K

CARD FUNCTIONS
U5
4145f023a
AA_GAYLE

_CC_CD(1)
_CC_CD(2)
_CC_BVD(1)
_CC_BVD(2)
_CC_WP
_CC_BUSY_IREQ
_REG
_WAIT
_IORD
_IOWR
_OE
_WE
_CC_ENA
CC_A0
CC_RESET

PE5
PE12
NOISE

C711 0.22uF

_IDE_IRQ
_IDE_CS(1)
_IDE_CS(2)
_INT2
_INT6

R715Y 10K

R715X 4.7K

U43 C43 0.22uF

U45 C45 0.22uF

U46 C46 0.22uF

U47 C47 0.22uF

A1200 Rev 1->1d PCB

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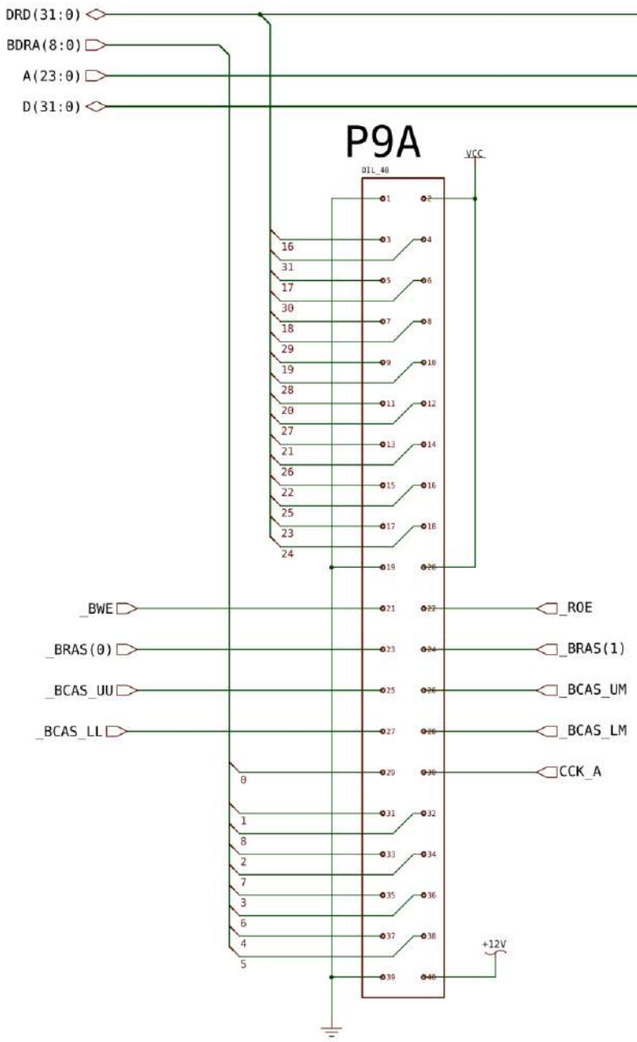
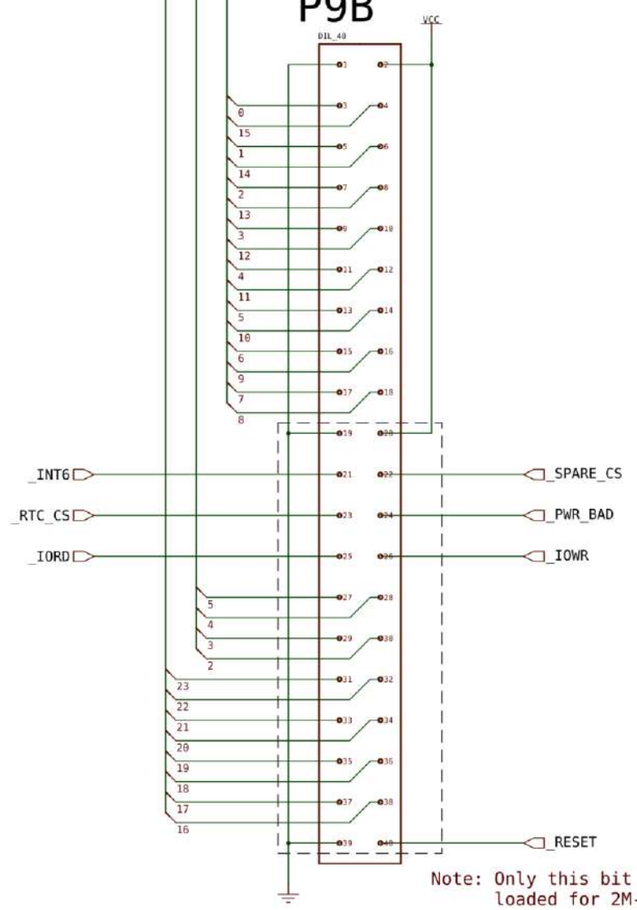
THE KISSY FACE CREDIT CARD MONSTER

Commodore
Schematic A1200 R1d
C/A1200 Main Board
"Channel Z"
SIZE C 364717 REV 1a
SCALE
SHEET 11 OF 13

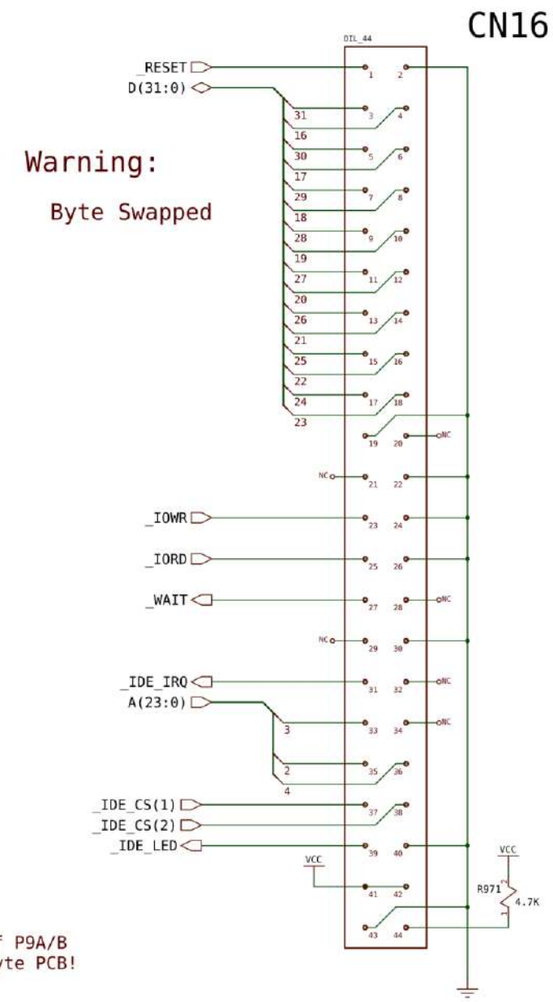
MEMORY EXPANSION





Note: Only this bit of P9A/B loaded for 2M-byte PCB!

IDE DRIVE



A1200 Rev 1->1d PCB

MEMORY EXPANSION AND THE IDE DRIVE

C.A.D. Generated
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DESIGN BY: C. Robbins	DATE 01/31/92	Commodore
DRAW: GBR	01/31/92	"Schematic A1200 Rld C/A1200 Main Board "Channel Z"
CHKD:		
APPR:		
USED ON C/A1200	NEXT ASSY 364738	SIZE C 364717 REV 1a
		SCALE SHEET 12 OF 13

PATH: /project/a500/channel_z.rev1 sheet12

EXPANSION CONNECTOR

P1

A(31:0)
D(31:0)
VCC

_IPL(2:0)
FC(2:0)
_RST
_ECS
SIZE_1
_AS
R_W
_STERM
_DSACK_1
CPUCLK_A
_CDIS
DELETED R1B PCB
_CIIN
_CBREQ
_BR
_BGACK
_FPU_CS
CCK_A
_NET_CS
_RTC_CS
_REG
_WAIT
_IORD
_OE
_OVR
_ZORRO
_INT2
SYSTEM_1
SYSTEM_0
_CONFIG_OUT
_xRxD
LEFT

_IPEND
_HLT
_OCS
SIZE_0
_DS
_BEER
_AVEC
_DSACK_0
E
_RMC
_CIOUT
_CBACK
_BG
_BOSS
_FPU_SENSE
_RESET
_SPARE_CS
_FLASH
_CC_ENA
_KB_RESET
_IOWR
_WE
XRDY
_WIDE
_INT6
_xTxD
RIGHT

+12V
GROUND
-12V
AUDIO
EDGE_150

POWER INPUT

CN8
5-PIn SQ
LF1
LINE FILTER
LF1A
LF1B
LF1C
LF1D
FB
C800 0.01uF
C801 0.01uF
C802 0.01uF
C803 0.01uF
C804 0.22uF
C821 47uF
C822 47uF
C811 1000uF
+12V
-12V
VCC
GND
SH

NOTE: HEAVY LINES INDICATE A
SINGLE POINT CONNECTION

HOLES &c.

CN1
CN2
CN5
CN6
CN7
CN9
CN15
MT1
MT2
MT3
MT4
MT5
MT6
MT7
MT8
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11
V12
V13
V14
V15

TEST ACCESS

10-PIN SIL

TP1
CPUCLK
_AS
_DS
R_W
_DSACK_0
_DSACK_1
_ROMEN
_CDIS
_KB_RESET

TP2
CCK
CCKQ
_RAMEN
_REGEN
_BLS
_OEB
_RAS
_CAS
_DWE

TP3
RGA(8:1)
_DBR

System Configuration Bits

SYSTEM	1	0	CPU/CPUCLK
	0	0	EC020/14MHz
	0	1	020/14MHz
	1	0	030/14MHz
	1	1	030/>14MHz

TERMINATION

VCC
_HLT
_RST
SIZE_0
SIZE_1
R_W
_AS
_DS
_DSACK_0
_DSACK_1
_BEER
_AVEC
_CDIS
_BR
_IPL(2:0)
FC(2:0)
_INT6
_INT2
_OVR
XRDY
_ZORRO
_WIDE
4.7K
470
1K
R951A
R951B
R951C
R951D
R951E
R951F
R951G
R952A
R952B
R101
R103
R102
R104
R953A
R953B
R953C
R953D
R953E
R953F
R954A
R954B
R954C
R954D
R954E
R592

C.A.D. Generated
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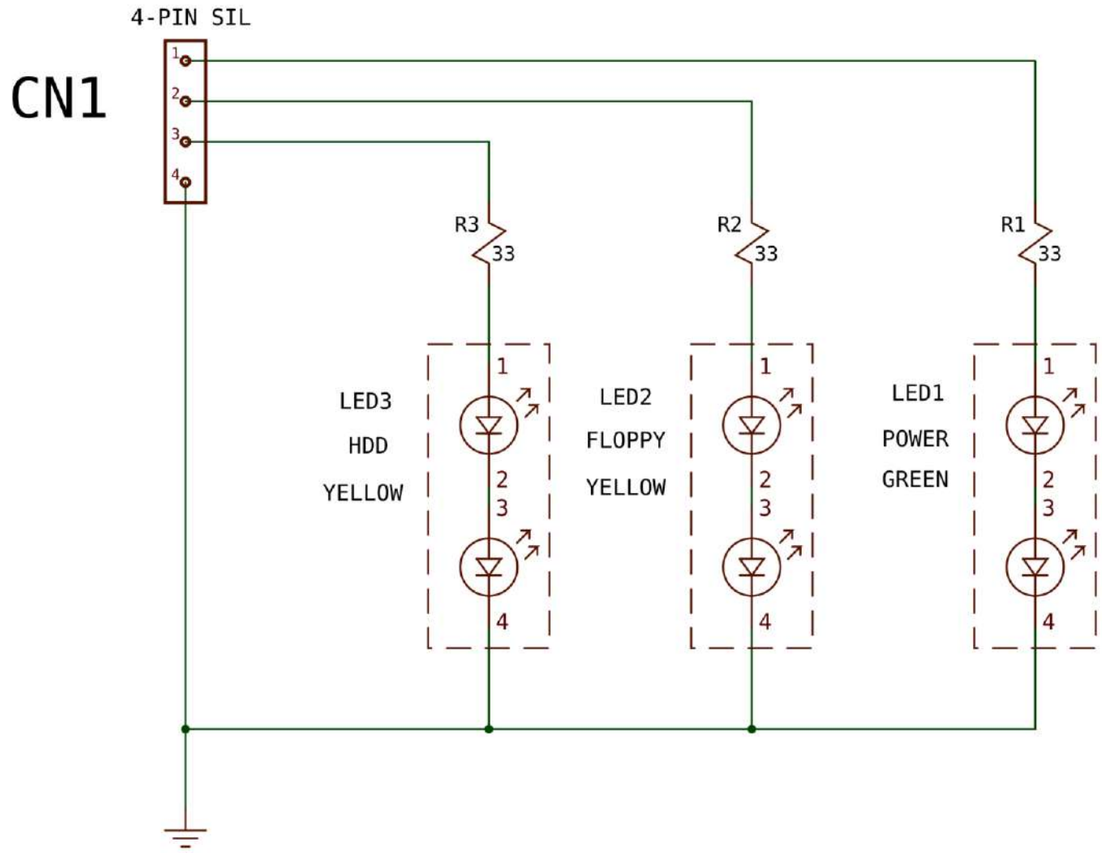
POWER DISTRIBUTION AND DECOUPLING

DESIGN BY: C. Rokosni 05/13/91
DRAW: GDB 03/13/91
CHKD:
APPR:
USED ON: C/A1200
NEXT ASSY: 364718

Commodore
Schematic A1200 R1d
C/A1200 Main Board
"Channel Z"
SIZE C 364717 REV 1a
SCALE
SHEET 13 OF 13
PATH: /project/a300/channel_z.rev1 sheet13

A1200 Rev 1->1d PCB

	REVISIONS			
REV	DESCRIPTION	DATE	APRVL	MANAGER
1	ADVANCE ENGINEERING RELEASE			



A1200 LED PCB ASSEMBLY REV1

SHINE ON, SHINE ON

C.A.D. Generated
No manual changes may be made to this document

	DESIGN BY:	DATE
	B. FENIMORE	7/21/92
	DRAW: BAF	7/21/92
	LAST: BAF	7/21/92
	CHKD:	
	APPR:	

USED ON	NEXT ASSY
A1200	364963

Commodore
SCHEMATIC
A1200 LED ASSY

SIZE		REV
A	364966	1
SCALE	SHEET 1 OF 1	

PATH: /user/fenimore/AA600/led assy sheet1