COMMODORE AMIGA A1200

Schematics

rev 2 www.amigawiki.org

Revision History

REV	DESCRIPTION	DATE	APRVL	MANAGER
0	Engineering Prototype	03/13/92	GRR	
1	Advance Engineering Release	06/29/92	GRR	
A	Production Release			

Jumpers and Stuff

REF	TYPE	DESCRIPTION	PAGE
R246	SMT	NTSC Color Burst	4
R202	SMT	PAL Color Burst	4
R625	SMT	Keyboard MPU Clock	9
R624	SMT	Keyboard/System Reset	9

Connectors

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	Mouse/Joystick 1	5
CN2	DB9P	Mouse/Joystick 2	5
CN3	RCA-J	Right Audio Output	5
CN4	RCA-J	Left Audio Output	5
CN5	DB23S	External Floppy	8
CN6	DB25P	RS232 Serial Port	7
CN7	DB25S	Parallel Printer Port	7
CN8	SQ DIN	Power Supply Connector	13
CN9	DB23P	Video Output	6
CN10	RCA-J	Composite Video	4
CN11	DIL-34	Internal Floppy Signal	8
CN12	SIL-4	Internal Floppy Power	8
CN13	MEM-30	Keyboard Membrane	9
CN14	SIL-4	Internal Floppy Power	8
CN13	MEM-30	Keyboard Membrane	9
CN14	SIL-4	Keyboard Status LED's	9
CN15	PCMCIA	PC"Memory Card"	11
P9	EDGE-80	Memory Bus Expansion	12

Signal Glossary

SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHz Master Clock	
7MHZ	7.15909 MHz Processor Clock	
A[23:1]	Processor Address Bus (68000)	
ACK	Data Acknowledge (Parallel Port)	
AS	Address Strobe (68000)	
AUDIN	Audio Input (RS232 Port)	
AUDOUT	Audio Output (RS232 Jack)	
BEER	Bus Error (68000)	
BG	Bus Grant (68000)	
BGACK	Bus Grant Acknowledge (68000)	
BLISS	Blitter Slowdown (Chips)	
BLIT	Chip Memory Access (Chips)	
BR	Bus Request (68000)	
BUSY	Device Busy (Parallel Port)	
CASL/U	Column Address Strobe (DRAM)	
CCK/CCKQ	Color Clock / Quadrature (Chips)	
CDAC	7.15909 MHz Quadrature Clock (Chips)	
CHNG	Media Change (Floppy)	
CLKRD/WR	Read-Time Clock Read / Write (RTC)	
COMP	Monochrome Composite Video (Video)	
CSYNC	Composite Sync (Video)	
CTS	Clear to Send (RS232 Port)	
D[15:0]	Processor Data Bus (68000)	
DIR	Step Direction (Floppy)	
DKRD	Disk Read Data (Floppy)	
DKWD	Disk Write Data (Floppy)	
DKWE	Disk Write Enable (Floppy)	
DMAL	Chip DMA Request Line (Chips)	
DRA[8:0]	DRAM Address Bus (DRAM)	
DRD[15:0]	DRAM Data Bus (DRAM)	
DSR	Data Set Ready (RS232 Port)	
DTACK	Data Transfer Acknowledge (68000)	
DTR	Data Terminal Ready (RS232 Port)	
E	Peripheral Enable Clock (68000)	
EXTICK	Expansion Present / RTC Tick	
FC[2:0]	Function Code (68000)	
FIRE0/1	Fire Button 0/1 (Joysticks)	
HLT	Processor Halt (68000)	
HSYNC	Horizontal Sync (Video)	
INDEX	Index Pulse (Floppy)	
INT[2,3,6]	Interrupt Request (Chips)	
IORESET	I/O Reset	
IPL[2:0]	Interrupt Priority Level (68000)	
KBCLOCK	Keyboard Clock (Keyboard)	
KBDATA	Keyboard Data (Keyboard)	
KBRESET	Keyboard Reset (Keyboard)	
LDS/UDS	Upper / Lower Data Strobes (68000)	
LED	Power On LED / Audio Filter Disable	
LEFT/RIGHT	Left Right Audio (Audio)	

SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	Light Pen Trigger (Joysticks)	
MTR	Motor On (Floppy)	
MTR0	Motor On - Drive 0 (Floppy)	
M0V/M0H	Mouse 0 Quadrature V/H (Joysticks)	
M1V/M1H	Mouse 1 Quadrature V/H (Joysticks)	
OVL	Overlay ROM over RAM	
OVR	Override System Decoding	
PIXELSW	Genlock Pixel Switch (Video)	
POT0X/0Y	Pot Lines 0 X/Y (Joysticks)	
POT1X/1Y	Pot Lines 1 X/Y (Joysticks)	
POUT	Paper Out (Parallel Port)	
PPD[7:0]	Parallel Port Data (Parallel Port)	
RAMEN	RAM Enable (Chips)	
REGEN	Chip Register Enable (Chips)	
RAS0/1	Row Address Strobe (DRAM)	
RDY	Drive Ready (Floppy)	
RESET	General Reset	
RGA[8:1]	Register Address Bus (Chips)	
R/G/B	Red / Green / Blue (Video)	
RI	Ring Indicate (RS232 Port)	
ROMEN	ROM Enable (ROM)	
RTS	Request to Send (RS232 Port)	
RST	Processor Reset (68000)	
RXD	Receive Data (RS232 Port)	
RW	Processor Read/Write (68000)	
SEL	Select (Parallel Port)	
SEL[3:0]	Drive Select (Floppy)	
SIDE	Side Select (Floppy)	
STEP	Step In/Out Command (Floppy)	
TRK0	Track Zero Sense (Floppy)	
TXD	Transmit Data (RS232 Port)	
VMA	Valid Memory Address (68000)	
VPA	Valid Peripheral Address (68000)	
VSYNC	Vertical Sync (Video)	
WE	Write Enable (DRAM)	
WPROT	Write Protect Sense (Floppy)	
XCLK	External Genlock Clock (Video)	
XCLKEN	External Clock Enable (Video)	
XRDY	External Data Ready	
	** Credit Card and IDE Stuff? **	

Key Components

REF	CHIP	DESCRIPTION	PAGE
U1	68EC020	68EC020 uP/16MHz	2
U2	8374	Alice (AA Agnus)	2
U3	8364	Paula	5
U4	4203	Lisa (AA Denise)	4
U5	f0022x	AA Gayle (CBM ASIC)	2,8,11
U6A-B	asst	ROM 512Kx16, 150 nS	10
U7-8	8520	Amiga VIA, 1 MHz	7
U10-11	28F400	4Mbit FLASH Memory	10
U12	CXA1145	Sony Video Encoder	4
U13	6570-36	Amiga Keyboard MPU	9
U14	NE555	Reset Timer	9
U15	LF347	BiMOS Op-Amp	5
	TL084	BiCMOS Op-Amp	alt
U16-17	Asst	DRAM 512Kx8, 80nS	3
U18-19	Asst	DRAM 512Kx8, optional	3
U20	391???	Bridgette (NCR ASIC)	2
U28	1488	EIA Line Driver	7
U29	1489	EIA Line Receiver	7
U30	BT101	Triple 8-bit Video DAC	4
X1	OSC	TTL 28.63636 MHz NTSC	2
	OSC	TTL 28.37512 MHz PAL	alt
Y451	XTAL	4.433619MHz PAL Burst	4
Y621	XTAL	3MHz Ceramic Resonator	9
X2	UD3626	PAL Video Modulator	4
	VA3424	NTSC Video Modulator	4

A1200 Rev 2 PCB

DIRECTORIES AND REVISION HISTORY

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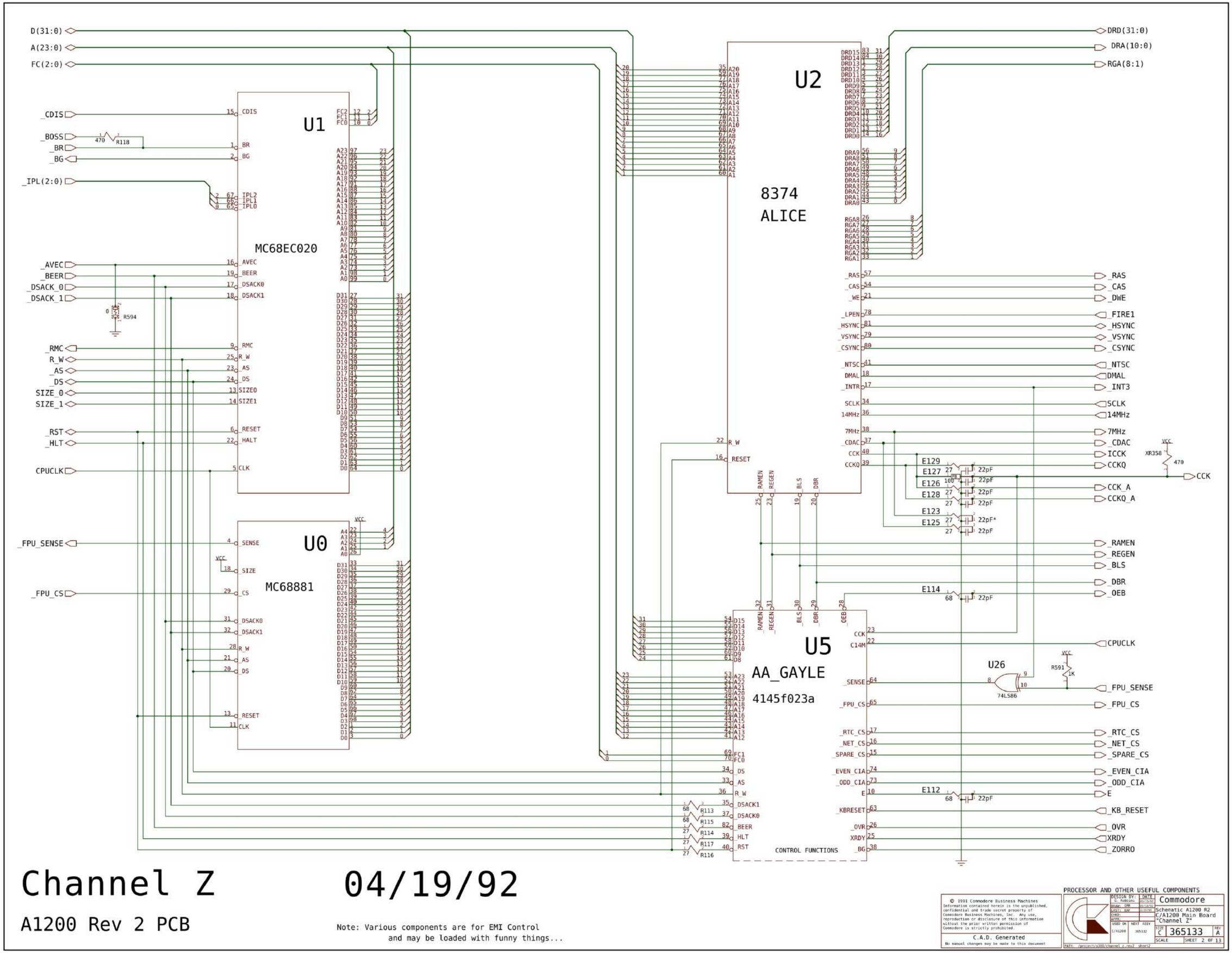
		DATE
DESIGN BY:	G. Nakajima	05/15/92
DRAW:	GRR	06/15/92
CHK1:	RAF	07/15/92
CHK2:		
APPR:		

USED ON: C/A1200 NEXT ASSY: 365132

Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"

SIZE C 365133 REV A
SCALE SHEET 1 OF 13

PATH: /project/a300/channel_z/rev2 sheet1



Channel Z

A1200 Rev 2 PCB

04/19/92

Note: Various components are for EMI Control
and may be loaded with funny things...

PROCESSOR AND OTHER USEFUL COMPONENTS

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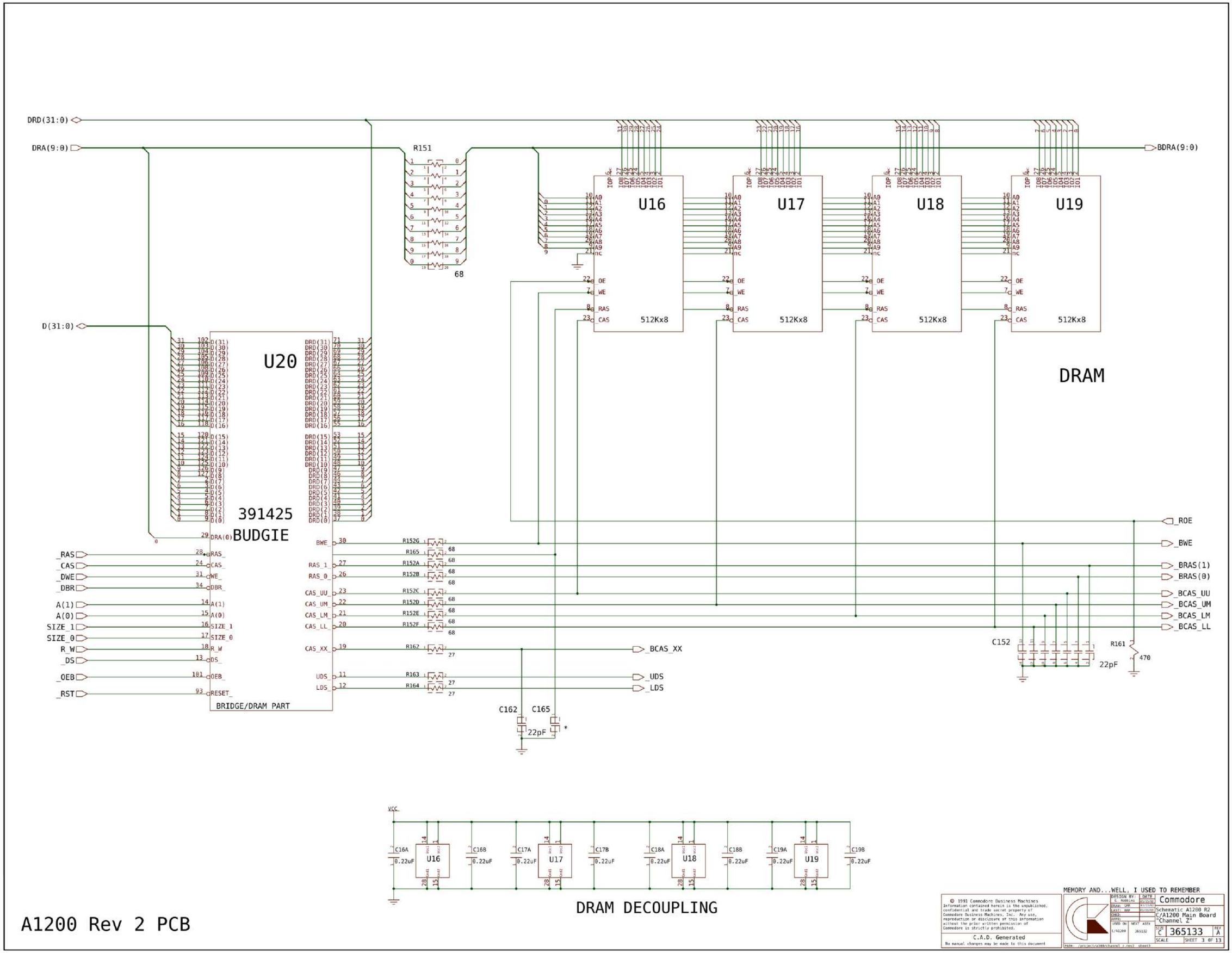
		DATE
DESIGN BY:	S. Nakajima	05/15/92
DRAW:	CRB	01/14/92
CHK1:	BAF	01/29/92
CHK2:		
APPR:		

USED ON: C/A1200 NEXT ASSY: 365132

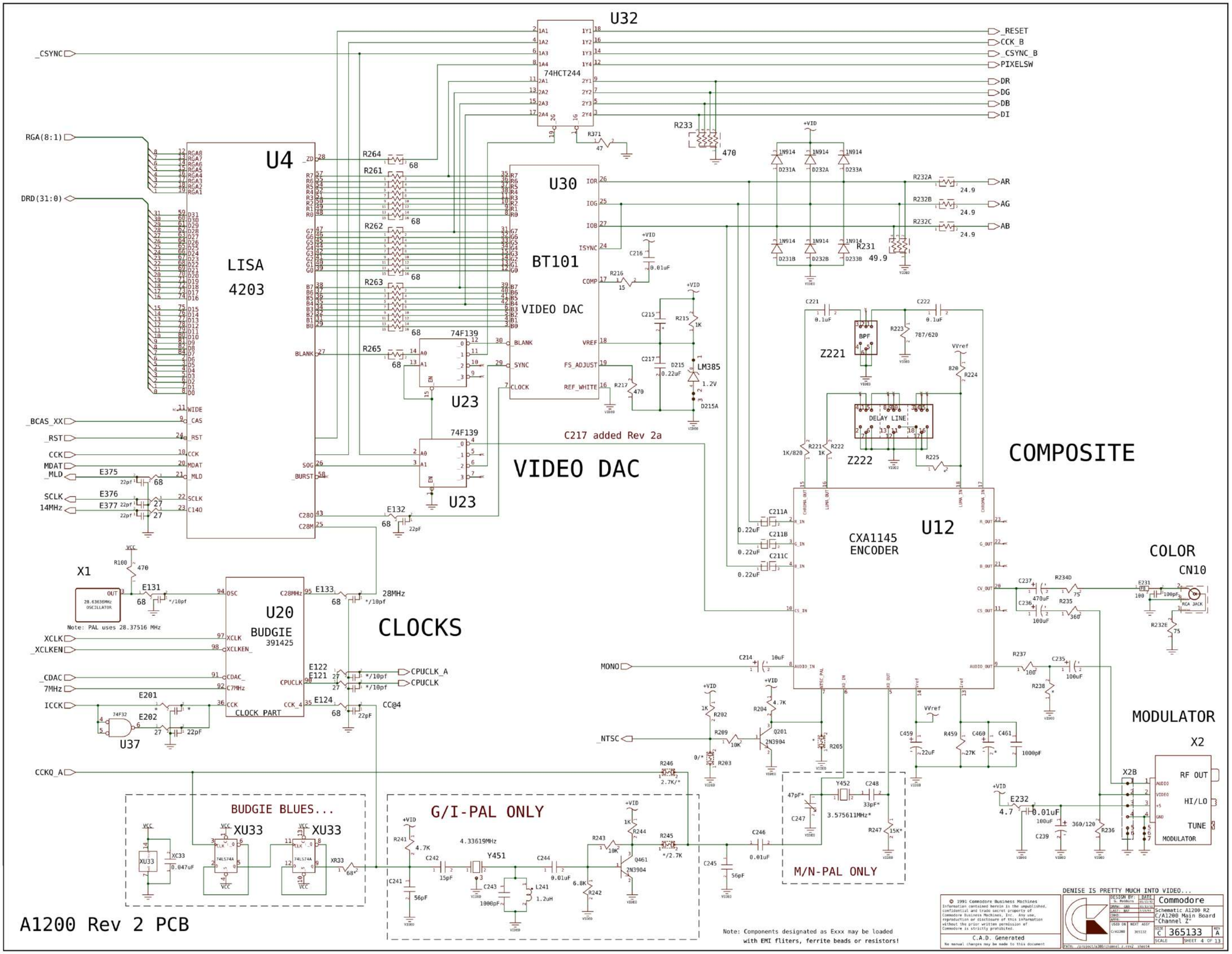
Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"

SIZE C 365133 REV A
SCALE SHEET 2 OF 13

PATH: /project/a300/channel_z.rev2 sheet2



A1200 Rev 2 PCB


U32
74HCT244
_CSYNC
_RESET
CCK_B
_CSYNC_B
PIXELSW
DR
DG
DB
DI
RGA(8:1)
DRD(31:0)
U4
LISA
4203
U30
BT101
VIDEO DAC
74F139
U23
C217 added Rev 2a
VIDEO DAC
_BCAS_XX
_RST
CCK
MDAT
_MLD
SCLK
14MHz
X1
28.63636MHz
OSCILLATOR
Note: PAL uses 28.37516 MHz
U20
BUDGIE
391425
CLOCK PART
CLOCKS
28MHz
XCLK
_XCLKEN
_CDAC
7MHz
ICCK
U37
CPUCLK_A
CPUCLK
CC@4
CCKQ_A
BUDGIE BLUES...
XU33
G/I-PAL ONLY
4.33619MHz
Y451
M/N-PAL ONLY
3.575611MHz*
MONO
_NTSC
Z221
Z222
DELAY LINE
CXA1145
ENCODER
U12
COMPOSITE
COLOR
CN10
RCA JACK
MODULATOR
X2
RF OUT
HI/LO
TUNE
MODULATOR
Note: Components designated as Exxx may be loaded
with EMI fliters, ferrite beads or resistors!
DENISE IS PRETTY MUCH INTO VIDEO...
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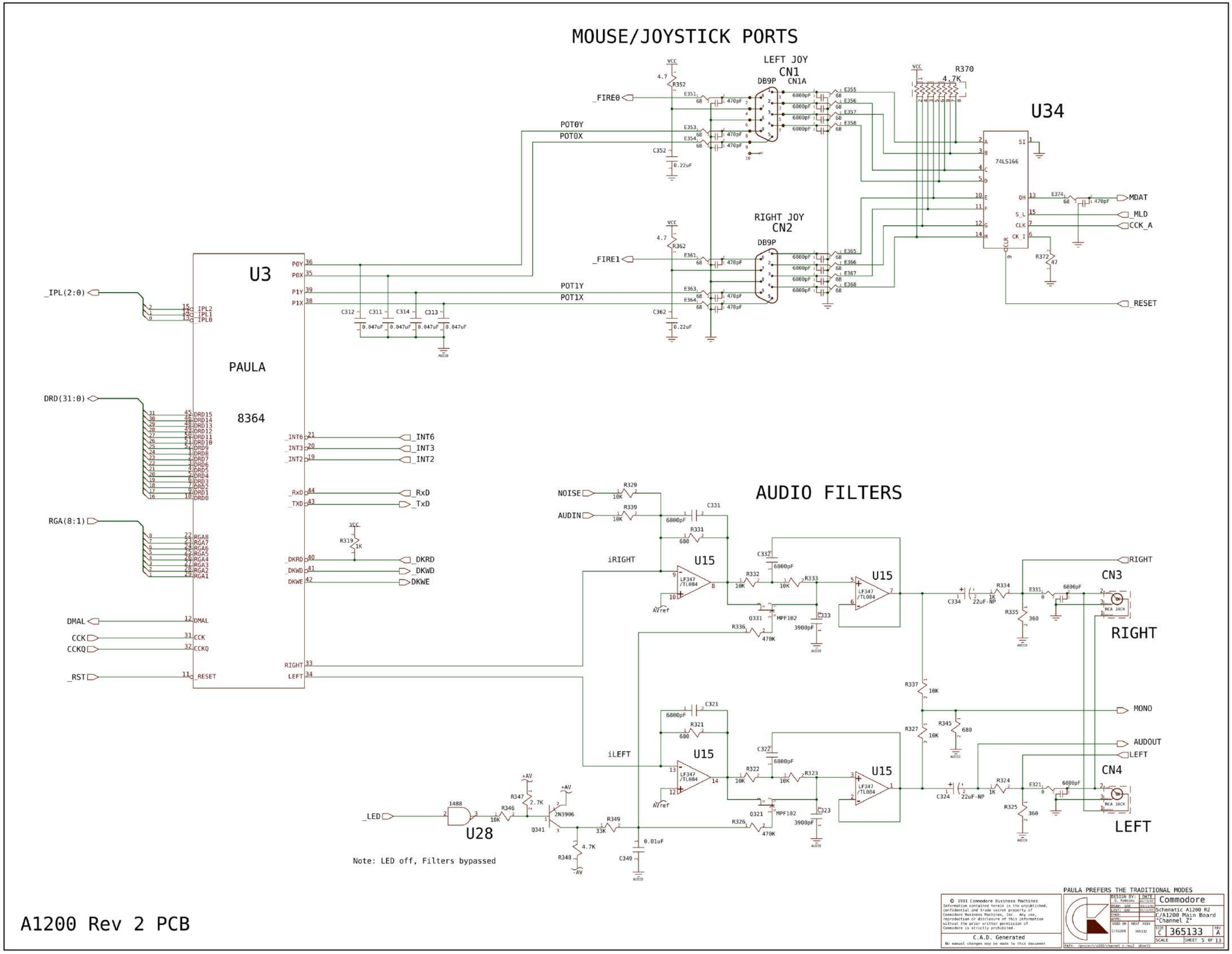
Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"
365133
SHEET 4 OF 13
A1200 Rev 2 PCB


MOUSE/JOYSTICK PORTS
LEFT JOY
CN1
DB9P
CN1A
RIGHT JOY
CN2
DB9P
U34
74LS166
R370
4.7K
U3
PAULA
8364
POT0Y
POT0X
POT1Y
POT1X
_FIRE0
_FIRE1
_IPL(2:0)
DRD(31:0)
RGA(8:1)
DMAL
CCK
CCKQ
_RST
_INT6
_INT3
_INT2
_RxD
_TxD
_DKRD
_DKWD
DKWE
RIGHT
LEFT
MDAT
_MLD
CCK_A
_RESET
AUDIO FILTERS
NOISE
AUDIN
iRIGHT
iLEFT
U15
LF347 /TL084
AVref
MPF102
CN3
CN4
RCA JACK
RIGHT
LEFT
MONO
AUDOUT
_LED
U28
2N3906
Note: LED off, Filters bypassed
A1200 Rev 2 PCB
PAULA PREFERS THE TRADITIONAL MODES
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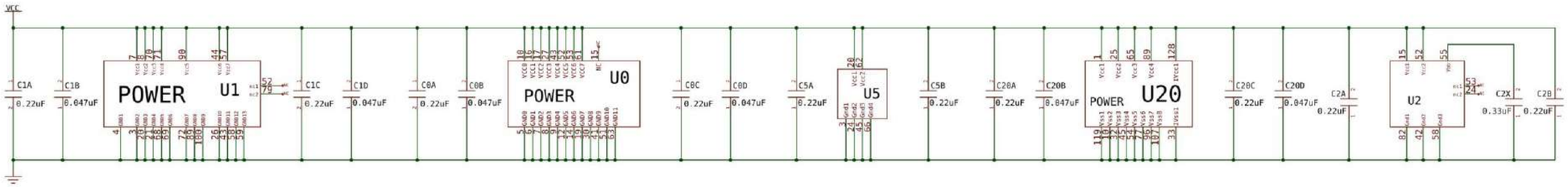
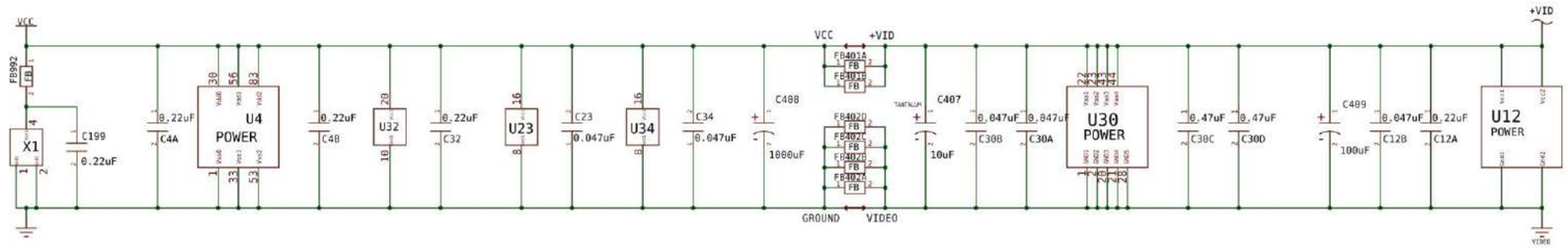
Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"
C 365133 A
SCALE
SHEET 5 OF 13

GENERAL DECOUPLING

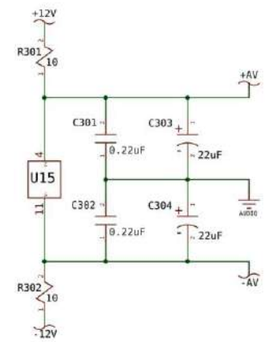


VIDEO DECOUPLING

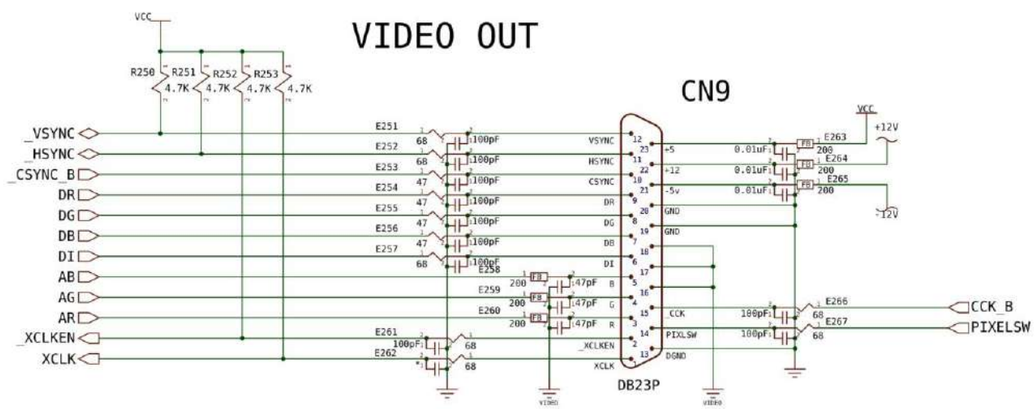


Note: Common Ground at DAC

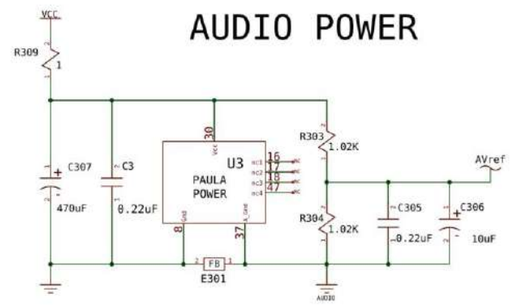
AUDIO DECOUPLING



VIDEO OUT



AUDIO POWER



Note: Common Ground near Jacks

A1200 Rev 2 PCB

PARTY OUT OF BOUNDS, WHAT A MESS...

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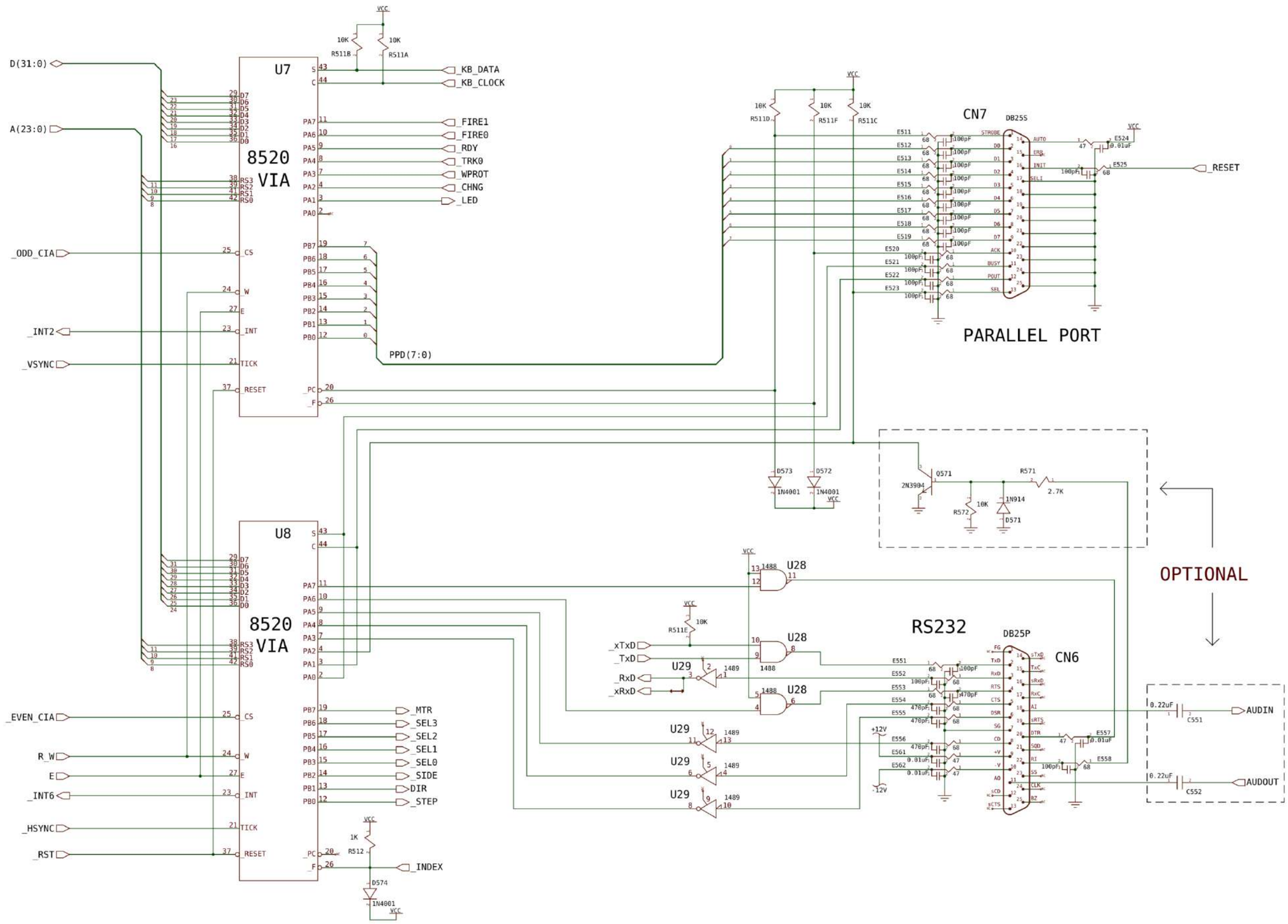
DESIGN BY: C. ROBBINS	DATE 02/15/92	Commodore
DRAW: GRR	02/15/92	Schematic A1200 R2
EAST: RRF	02/15/92	C/A1200 Main Board
CHKD:		"Channel Z"
APPR:		
USED ON C/A1200	NEXT ASSY 365132	SIZE C 365133 REV A
		SCALE SHEET 6 OF 13

PATH: /projects/a1200/channel_z/rev2 sheet6



A1200 Rev 2 PCB

SERIAL AND PARALLEL PORTS

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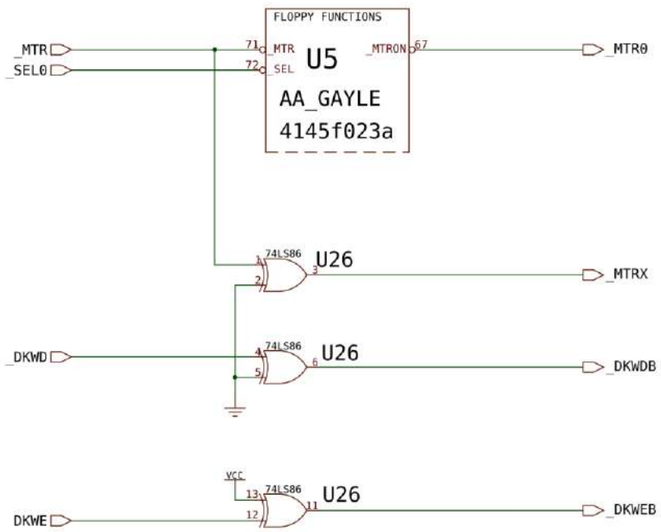
DESIGN BY:	DATE
C. Robbins	05/13/91
DRAW: GRB	12/12/91
CHKD: RAP	02/10/92
CHKD:	
APPR:	
USED ON: C/A1200	NEXT ASSY: 365132

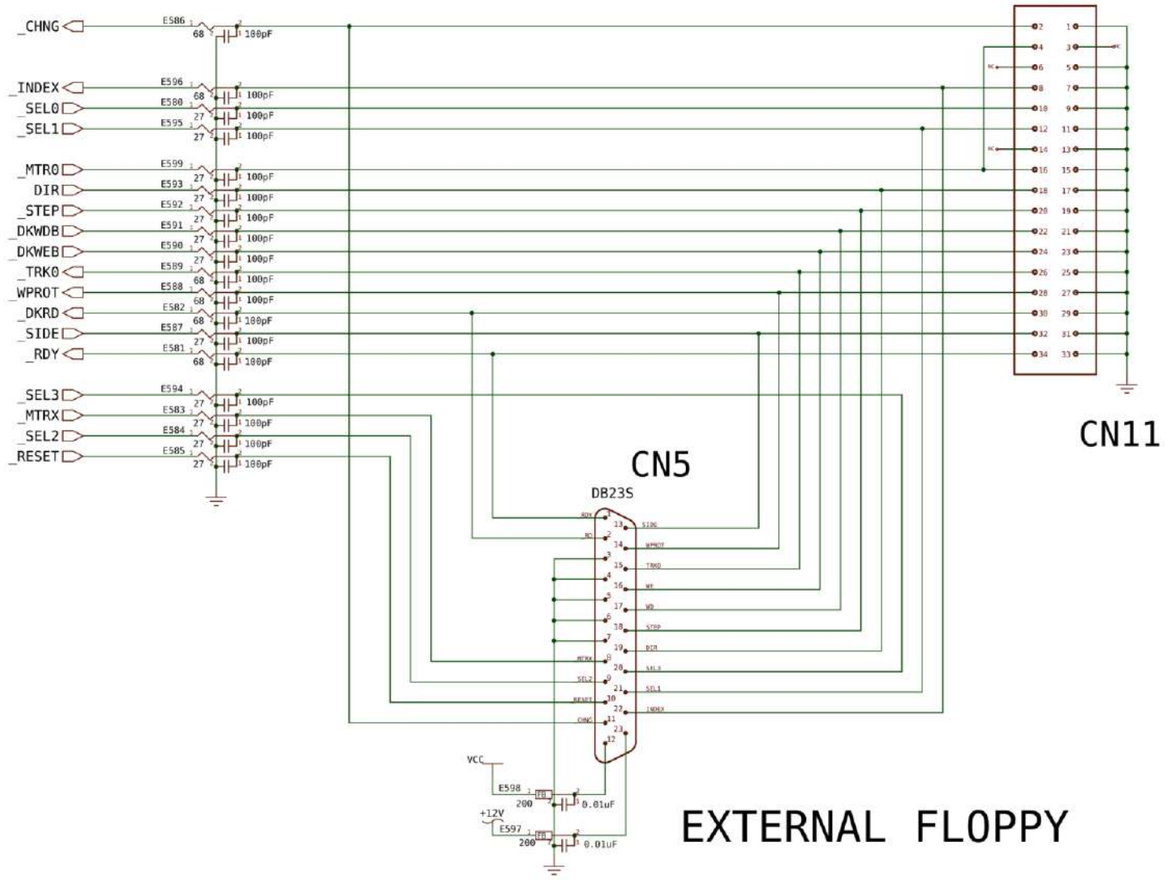
Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"

SIZE C | 365133 | REV A
SCALE | SHEET 7 OF 13
PATH: /projects/a1200/channel_z.rev2 sheet7

FLOPPY LOGIC

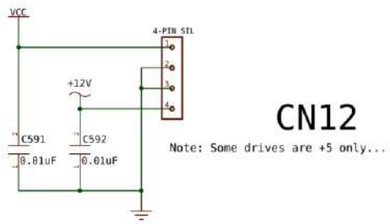


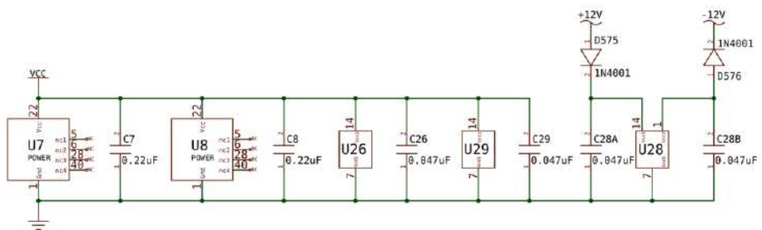
INTERNAL FLOPPY



EXTERNAL FLOPPY

FLOPPY POWER





DECOUPLING

A1200 Rev 2 PCB

THE REST OF THE FLOPPY STUFF

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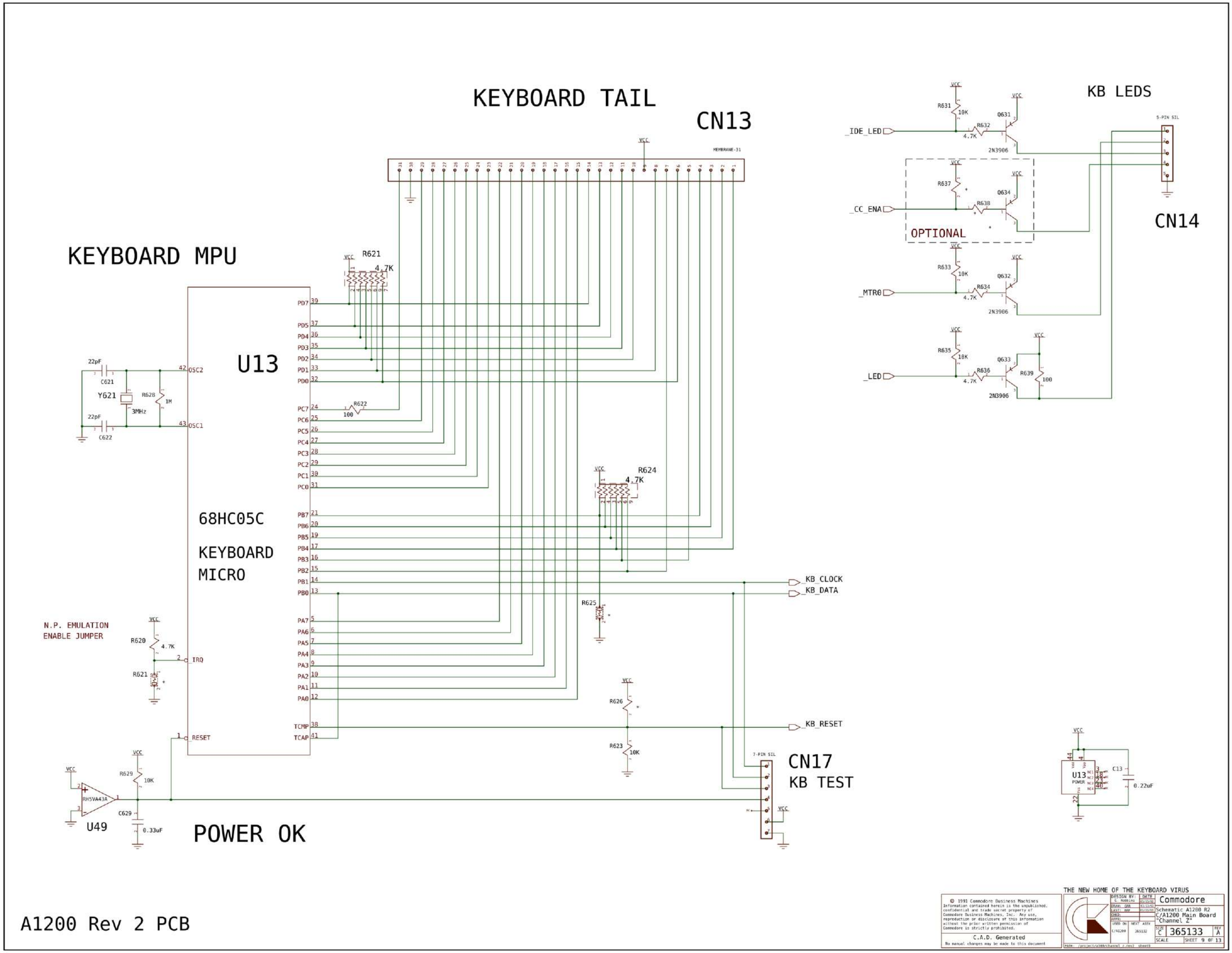
DESIGN BY	DATE
C. Robbins	02/15/92
DRAW: DRB	02/15/92
CHKD: MAP	02/15/92
CHKD:	
APPR:	
USED ON	NEXT ASSY
C/A1200	365132

Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"

SIZE C | 365133 | REV A
SCALE | SHEET 8 OF 13

PATH: /project/a1200/channel_z/rev2 sheet8



A1200 Rev 2 PCB

THE NEW HOME OF THE KEYBOARD VIRUS

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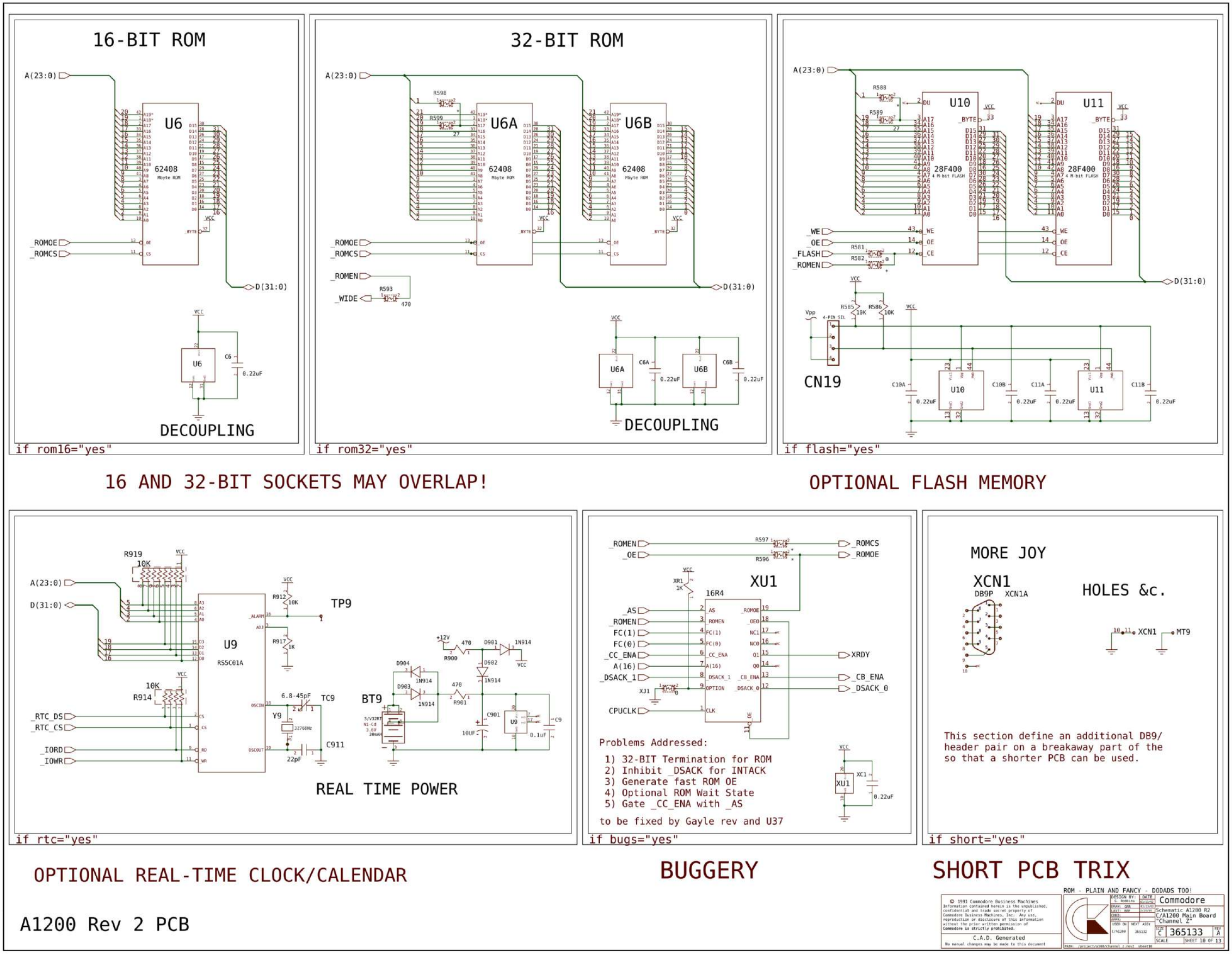
DESIGN BY: G. Robbins	DATE 03/15/92	Commodore
DRAW: GRR	03/15/92	Schematic A1200 R2
EAST: GRR	03/11/92	C/A1200 Main Board
DB2:		"Channel Z"
APPR:		
USED ON C/A1200	NEXT ASSY 365132	SIZE C 365133 REV A
		SCALE SHEET 9 OF 13

PATH: /project/a1200/channel_z/rev2 sheet9


16-BIT ROM
A(23:0)
U6
62408
8Byte ROM
ROMOE
_ROMCS
D(31:0)
VCC
C6
0.22uF
DECOUPLING
if rom16="yes"
32-BIT ROM
R598
R599
U6A
U6B
_ROMEN
_WIDE
R593
470
C6A
C6B
if rom32="yes"
U10
U11
28F400
4 M-bit FLASH
_WE
_OE
_FLASH
_ROMEN
R581
R582
R585
R586
10K
Vpp
4-PIN STL
CN19
C10A
C10B
C11A
C11B
if flash="yes"
16 AND 32-BIT SOCKETS MAY OVERLAP!
OPTIONAL FLASH MEMORY
R919
R914
U9
RS5C01A
_RTC_DS
_RTC_CS
_IORD
_IOWR
R912
R917
TP9
6.8-45pF
TC9
Y9
32768Hz
22pF
C911
BT9
R900
R901
D901
D902
D903
D904
1N914
C901
10UF
C9
0.1uF
REAL TIME POWER
if rtc="yes"
_ROMCS
_ROMOE
XU1
16R4
_AS
FC(1)
FC(0)
_CC_ENA
A(16)
_DSACK_1
CPUCLK
XRDY
_CB_ENA
_DSACK_0
XR1
XJ1
XC1
Problems Addressed:
1) 32-BIT Termination for ROM
2) Inhibit _DSACK for INTACK
3) Generate fast ROM OE
4) Optional ROM Wait State
5) Gate _CC_ENA with _AS
to be fixed by Gayle rev and U37
if bugs="yes"
MORE JOY
XCN1
DB9P
XCN1A
HOLES &c.
MT9
This section define an additional DB9/
header pair on a breakaway part of the
so that a shorter PCB can be used.
if short="yes"
OPTIONAL REAL-TIME CLOCK/CALENDAR
BUGGERY
SHORT PCB TRIX
ROM - PLAIN AND FANCY - DODADS TOO!
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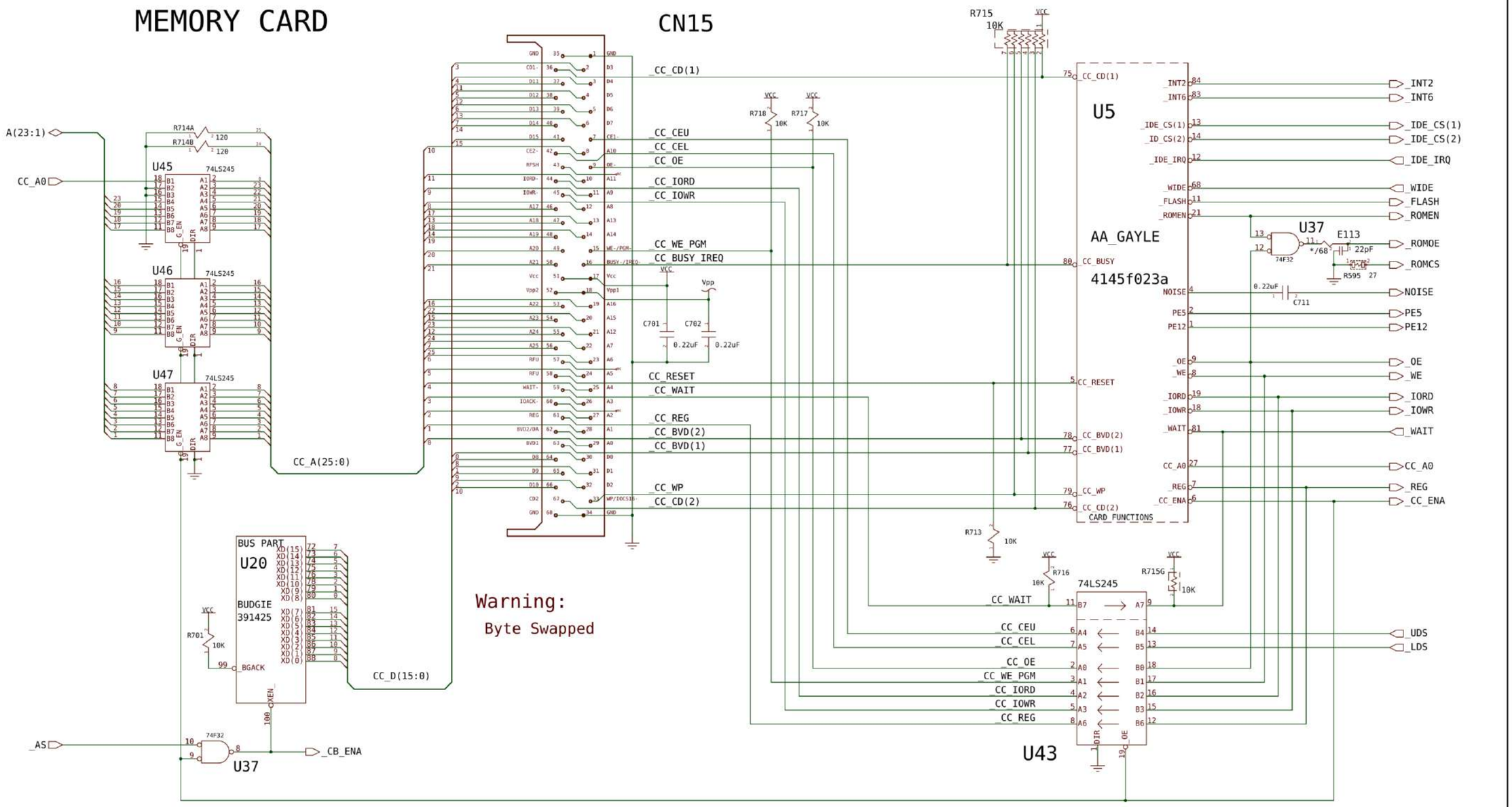
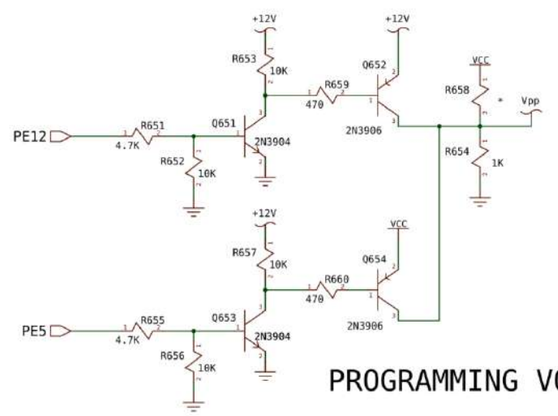
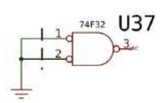
DESIGN BY
G. Robbins
DATE
DRAW: GRR
CHKD:
APPR:
USED ON
C/A1200
NEXT ASSY
365132
Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"
SIZE
C
365133
REV
A
SCALE
SHEET 10 OF 13
A1200 Rev 2 PCB

MEMORY CARD

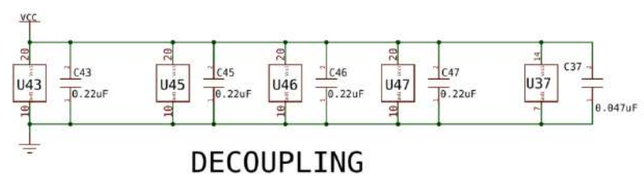




PROGRAMMING VOLTAGE



SPARE



DECOUPLING

A1200 Rev 2 PCB

THE KISSY FACE CREDIT CARD MONSTER

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C.A.D. Generated
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		DATE
DESIGN BY:	G. Robbins	01/15/92
DRAW:	GGR	02/14/92
ENG:	BAF	01/15/92
CHKD:		
APPR:		

Commodore
Schematic A1200 R2
C/A1200 Main Board
"Channel Z"

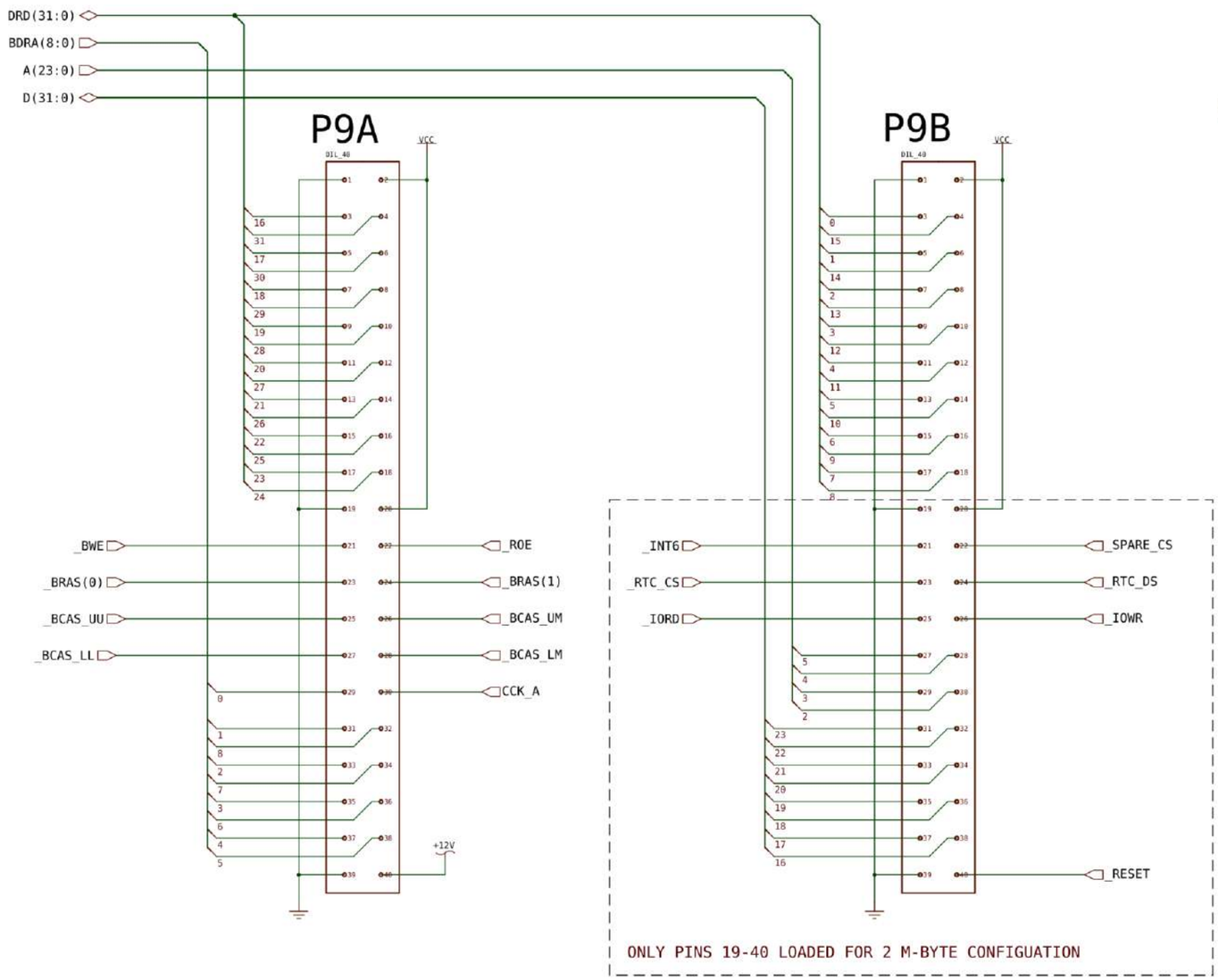
USED ON: C/A1200 | NEXT ASSY: 365132

SIZE C | 365133 | REV A

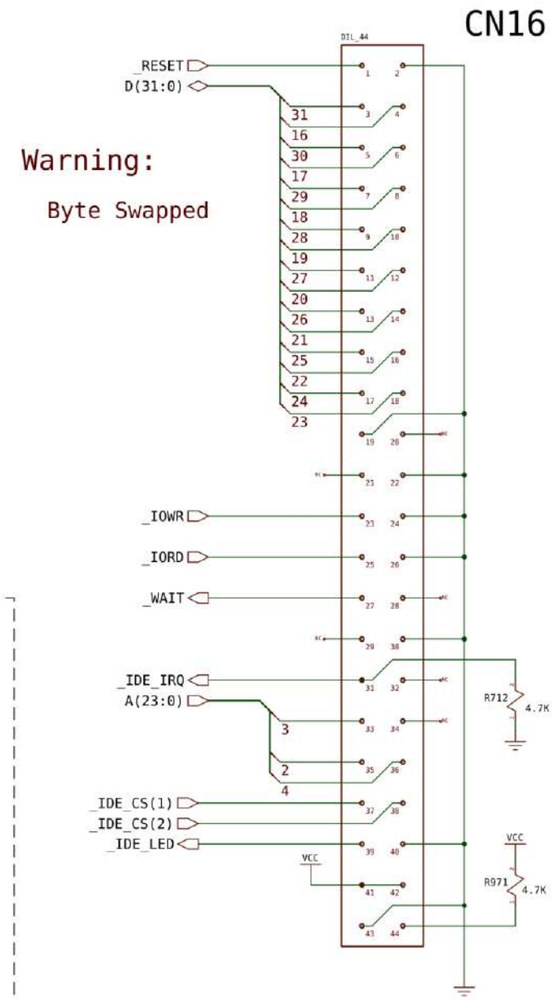
SCALE | SHEET 11 OF 13

PATH: /project/a500/channel_z/rev2 sheet11

MEMORY EXPANSION



IDE DRIVE



A1200 Rev 2 PCB

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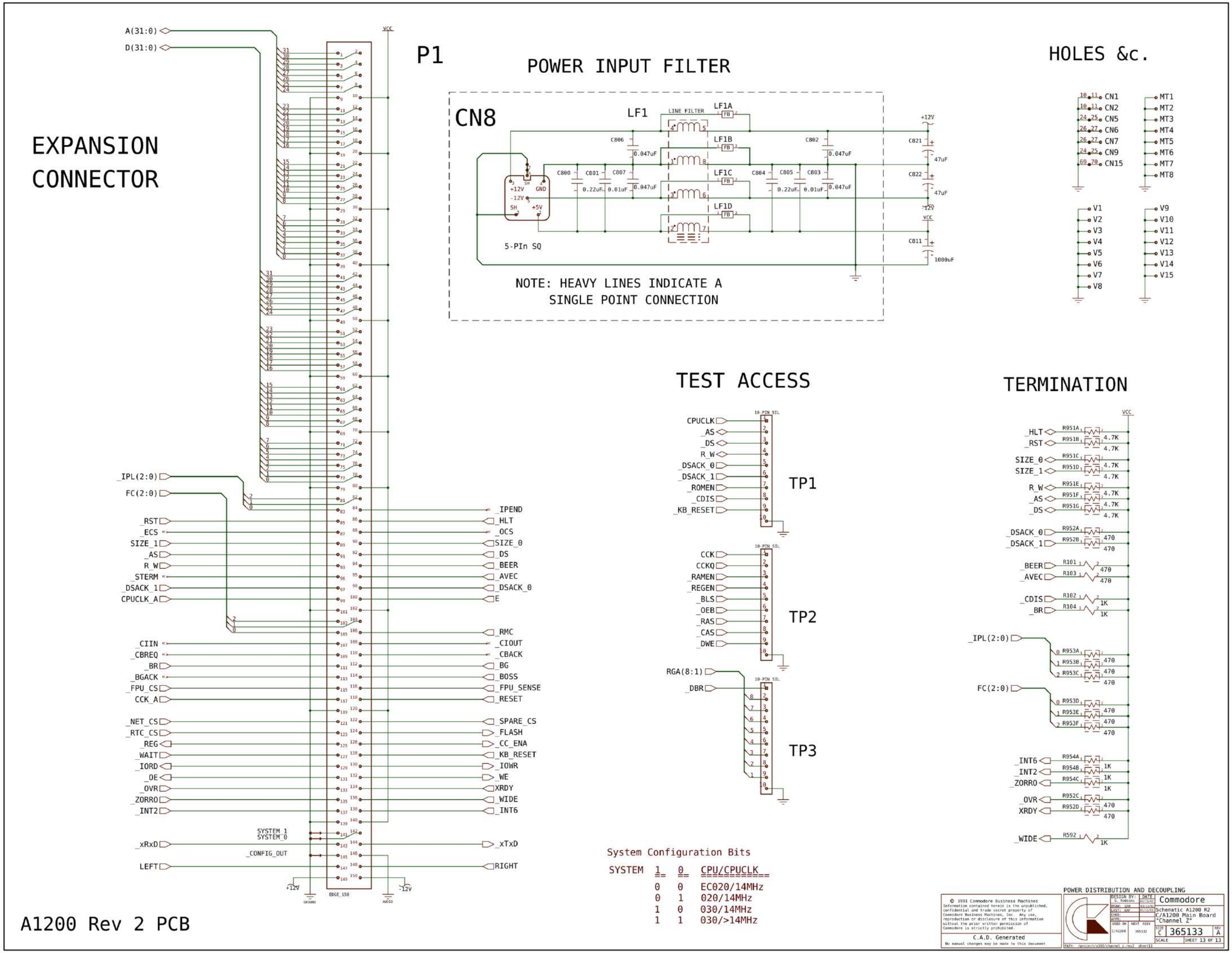
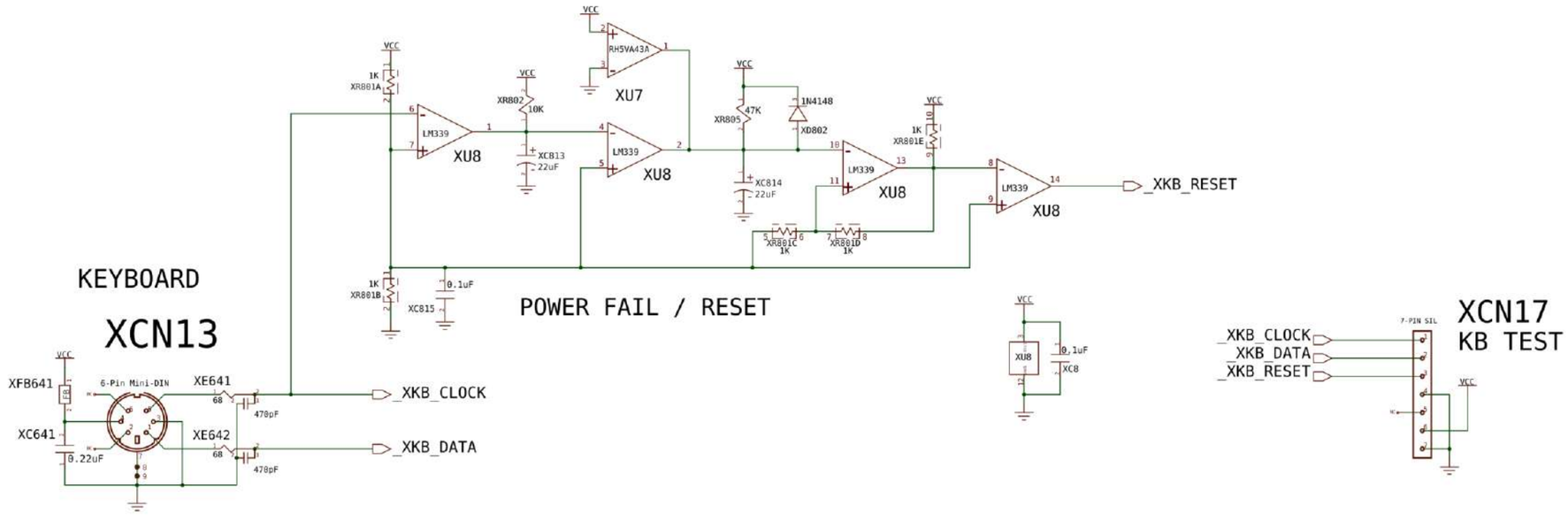
MEMORY EXPANSION AND THE IDE DRIVE

DESIGN BY: G. ROBBINS	DATE 01/15/92	Commodore
DRAW: GRB	01/15/92	Schematic A1200 R2
LAST: MRP	01/15/92	C/A1200 Main Board "Channel Z"
CHKD:		
APPR:		
USED ON: C/A1200	NEXT ASSY: 265132	SIZE C 365133 REV A
		SCALE SHEET 12 OF 13

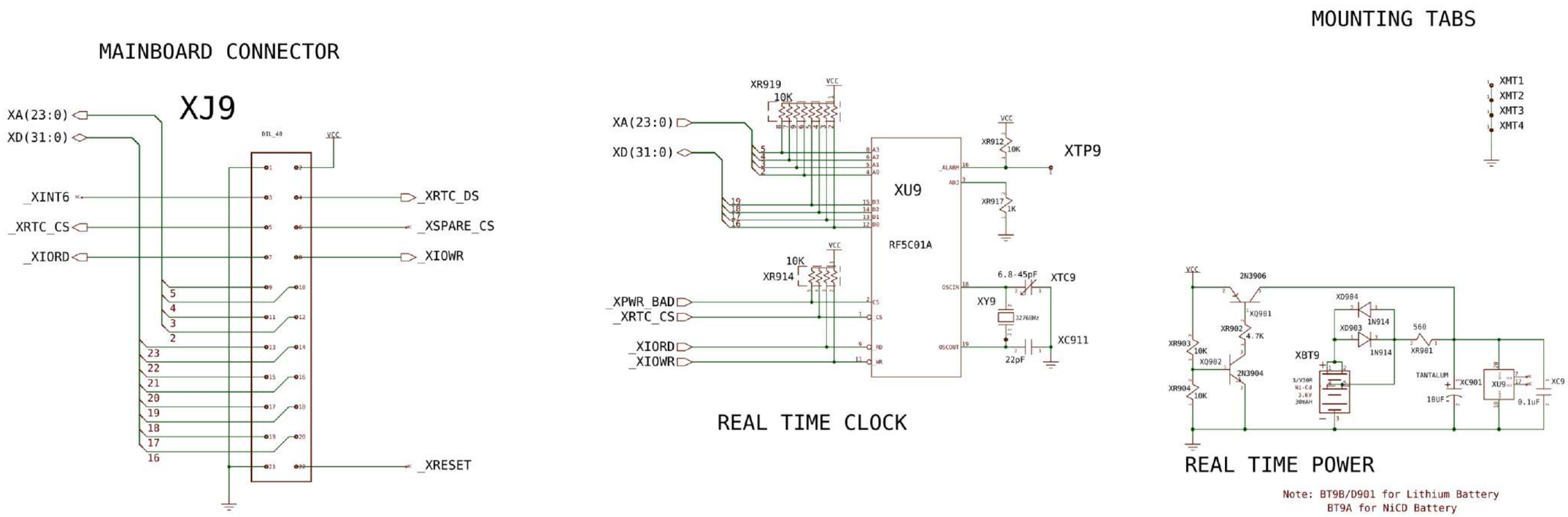
PATH: /project/a1200/channel_z/rev2 sheet12



A1200 Rev 2 PCB



IF KBTEST="YES"



IF EXTRTC="YES"

A1200 Rev 2 PCB

BREAKAWAY PCB RTC OPTION

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DESIGN BY: G. Robbins	DATE 03/15/92	Commodore
DRAWN: GRR	03/15/92	Schematic A1200 R2
CHKT: GRR	04/09/92	C/A1200 Main Board
CHKD:		"Channel Z"
APPR:		
USED ON: C/A1200	NEXT ASSY: 364738	SIZE C 364717 REV 2
		SCALE SHEET 14 OF 13

PATH: /project/a1200/channel_z.rev2 sheet13