TI-99/4A CONSOLE TECHNICAL DATA

1049716-2

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A. TI-99/4A CONSOLE TECHNICAL DATA

A.1 GENERAL DESCRIPTION

The purpose of this manual is to provide necessary information concerning the I/O bus (input/output signal connection) of the TI-99/4A console for persons interested in designing peripherals for the computer. Also included are the description and schematics of the modified Home Computer console called the TI-99/4QI. Both the 99/4A and the 99/4QI function almost identically. Throughout the text, references to the 99/4A are applicable to the 99/4QI. Schematics and component placement diagrams are specifically labeled as either 99/4A or 99/4QI.

It is assumed that readers of this manual have a working knowledge of electronics and computers, especially in regard to the TMS 9900 microprocessor and its Communications Register Unit (CRU) I/O technique. Sources for this information are the TMS9900 Microprocessor Data Manual (MP001, Revision A) or the TMS9901 Programmable Systems Interface (MP003; July, 1978). These books may be obtained from TI semiconductor distributors or the TI Learning Center. A glossary is provided on page 19 of this manual.

The I/O bus provides an interface between the console and its peripherals. This bus utilizes both memory-mapped I/O and CRU I/O. The memory bus is frequently used for instruction fetch from read-only memory (ROM) in external peripherals and for data transfer to and from memory-mapped portions of these devices. The CRU bus is used for peripheral enable/disable, device control, and data transfer to/from CRU-mapped portions of these peripherals.

The TMS 9900 microprocessor accesses each peripheral to obtain instructions from the device service routine (DSR) ROM. Since each peripheral contains its own DSR, the TI-99/4A does not have to be designed to anticipate future peripheral requirements. The dual I/O bus capability, interrupt handling, and external DSRs provide flexibility at low cost.

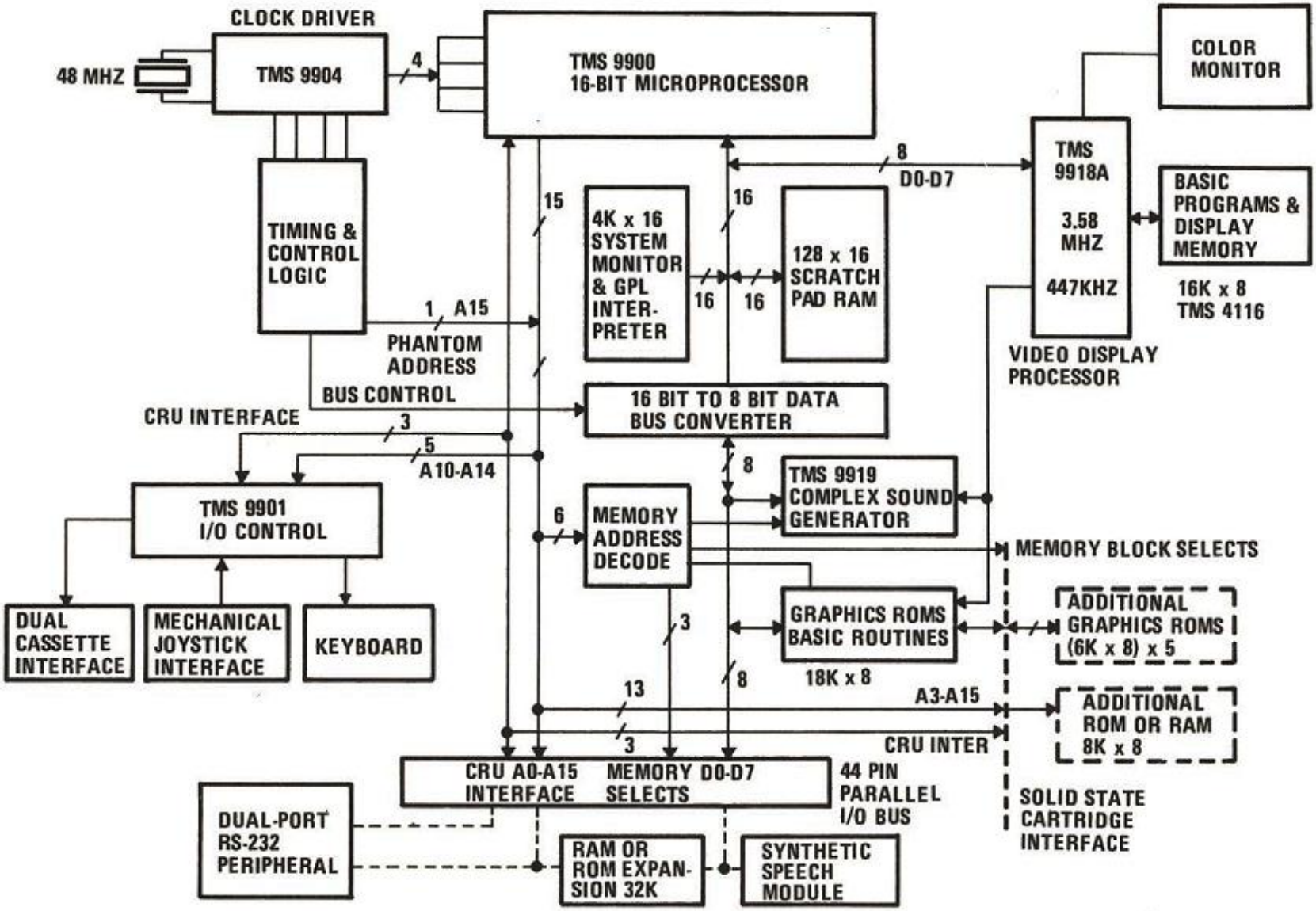


FIGURE A. TI-99/4A SYSTEM BLOCK DIAGRAM

A.2 I/O PIN DESCRIPTION

SIGNATURE	PIN	I/O	DESCRIPTION
A0 (MSB)	31	Out	
A1	30	Out	ADDRESS BUS
A2	20	Out	
A3	10	Out	A0 through A15 comprise the address bus.
A4	7	Out	This bus provides the 16-bit memory
A5	5	Out	address vector to the external memory
A6	29	Out	system when $\overline{\text{MEMEN}}$ is active. Address
A7	17	Out	bit 15 is also used for CRU DATA OUT
A8	14	Out	on CRU output instructions.
A9	18	Out	
A10	6	Out	
A11	8	Out	
A12	11	Out	
A13	15	Out	
A14	16	Out	
A15/CRUOUT	19	Out	
D0 (MSB)	37	I/O	DATA BUS
D1	40	I/O	
D2	39	I/O	D0 through D7 comprise the bidirectional
D3	42	I/O	data bus. This bus transfers memory data
D4	35	I/O	to (when writing) and from (when reading)
D5	38	I/O	the external memory system when $\overline{\text{MEMEN}}$ is
D6	36	I/O	active.
D7	34	I/O	
			BUS CONTROL
$\overline{\text{MEMEN}}$	32	Out	MEMory ENable. $\overline{\text{MEMEN}}$ indicates a memory access.
DBIN	9	Out	Data Bus IN. When active (high) the data buffers and 9900 are in the input mode.
$\overline{\text{WE}}$	26	Out	Write Enable. $\overline{\text{WE}}$ indicates a memory write.
$\overline{\text{MBE}}$	28	Out	Memory Block Enable. $\overline{\text{MBE}}$ indicates a memory access in memory block 4000-5FFF.
$\overline{\text{CRUCLK}}$	22	Out	CRU CLocK. Indicates a CRU Write operation.
CRUIN	33	In	CRU data IN. Input data line to the Home Computer.

I/O PIN DESCRIPTION (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
			MEMORY CONTROL
READY	12	In	READY (when $\overline{\text{MEMEN}}$ is active) indicates external memory is ready for a memory access.
IAQ	41	Out	Instruction AcQuisition indicates the CPU is acquiring an instruction during the current memory cycle.
			TIMING AND CONTROL
$\overline{\text{LOAD}}$	13	In	When active, $\overline{\text{LOAD}}$ causes the CPU to execute a nonmaskable interrupt; memory addresses FFFC and FFFE contain the new workspace and PC vectors, respectively.
$\overline{\text{RESET}}$	3	Out	When active, $\overline{\text{RESET}}$ causes the Home Computer and the peripherals to be reset. $\overline{\text{RESET}}$ will be held active for a minimum of five clock cycles.
$\overline{\text{EXT INT}}$	4	In	EXTernal INTerrupt. When active, $\overline{\text{EXT INT}}$ causes the CPU to execute an interrupt.
$\overline{\phi 3}$	24	Out	CPU Clock. Phase 3 of the CPU clock.
			POWER
GND	21,23 25,27		Ground reference.
			SPEECH MODULE SIGNALS
SBE	2	Out	Speech Block Enable. SBE indicates a memory access in the speech memory.
AUDIO IN	44	In	Input for the audio from the speech module
+5	1		Supply voltage (+5v Nom) for speech module (50ma Max)*
-5	43		Supply voltage (-5v Nom) for speech module (50ma Max)*

* NOTE: Pins 1 and 43 are not intended for use by consumer. Overload may cause permanent damage to console.

A.3 MEMORY ALLOCATION

The memory address space is broken into eight blocks of 8K bytes of memory. The third block (addresses 4000-5FFF) is predecoded and made available at the I/O port for the peripherals. The second, sixth, seventh, and eighth blocks (addresses 2000-3FFF and A000-FFFF) are in the Memory Expansion peripheral. For the speech module (addresses 9000-97FF), a predecoded line is available at the I/O port.

SYSTEM MEMORY MAP

HEX ADDRESS	
0-1FFF	Console ROM space
2000-3FFF	Memory Expansion Peripheral
4000-5FFF	Peripheral Expansion (predecoded to I/O connector)
6000-7FFF	Cartridge ROM/RAM (predecoded to GROM connector)
8000-9FFF	Microprocessor ROM, VDP, GROM, SOUND and SPEECH select.
A000-BFFF	Memory Expansion peripheral
C000-DFFF	Memory Expansion peripheral
E000-FFFF	Memory Expansion peripheral

MEMORY-MAPPED DEVICES

ADDRESSES	A0	A1	A2	A3	A4	A5	A14	USE
8000	1	0	0	0	0	0	0	Internal RAM (8300-83FF)
8400	1	0	0	0	0	1	0	Sound
8800	1	0	0	0	1	0	0	VDP Read Data
8802	1	0	0	0	1	0	1	VDP Read Status
8C00	1	0	0	0	1	1	0	VDP Write Data
8C02	1	0	0	0	1	1	1	VDP Write Address
9000	1	0	0	1	0	0	0	Speech Read
9400	1	0	0	1	0	1	0	Speech Write
9800	1	0	0	1	1	0	0	GROM Read Data
9802	1	0	0	1	1	0	1	GROM Read Address
9C00	1	0	0	1	1	1	0	GROM Write Data
9C02	1	0	0	1	1	1	1	GROM Write Address

NOTE: Memory-mapped devices at addresses >8000 through >9FFF are only partially decoded. Thus, the devices will respond not only at the base addresses listed above, but also at other addresses within the 1K block.

A.4 CRU ALLOCATION

Of the available 4K of CRU bits, the first 1K (addresses 0000-07FE) are used internally in the console. The second 1K (addresses 0800-0FFE) are reserved for future use. The last 1.9K (addresses 1000-1FFE) are reserved for the peripherals to be plugged in the I/O port. A block of 128 CRU bits is assigned to each peripheral as listed below.

CRU ASSIGNMENTS

CRU ADDRESSES	A3	A4	A5	A6	A7	USE
0000-0FFE	0	X	X	X	X	Internal Use
1000-10FE	1	0	0	0	0	Unassigned
1100-11FE	1	0	0	0	1	Disk Controller Card
1200-12FE	1	0	0	1	0	Reserved
1300-13FE	1	0	0	1	1	RS-232 (primary)
1400-14FE	1	0	1	0	0	Unassigned
1500-15FE	1	0	1	0	1	RS-232 (secondary)
1600-16FE	1	0	1	1	0	Unassigned
1700-17FE	1	0	1	1	1	HEX-BUS™ Interface
1800-18FE	1	1	0	0	0	Thermal Printer
1900-1FFE	1	1	0	0	0	Reserved
1A00-1AFE	1	1	0	1	0	Unassigned
1B00-1BFE	1	1	0	1	1	Unassigned
1C00-1CFE	1	1	1	0	0	Video Controller Card
1D00-1DFE	1	1	1	0	1	IEEE 488 Bus Controller Card
1E00-1EFE	1	1	1	1	0	Unassigned
1F00-1FFE	1	1	1	1	1	P-Code Card

A.5 INTERRUPT HANDLING

The interrupt available on the I/O port is one of the maskable interrupts of the TMS 9901 Programmable Systems Interface.

9900 INTERRUPTS

INTERRUPT LEVEL	VECTOR LOC. (MEMORY ADDR. IN HEX)	CPU PIN	DEVICE ASSIGNMENT
(Highest Priority)	0000-WSP 0002-PC	RESET	RESET
0	FFFC-WSP FFFE-PC	LOAD	LOAD
1	0004-WSP 0006-PC	--	EXT DEV (9901)

Interrupting is done only on Level 1. The additional interrupts available are implemented on 9901. Interrupt Level 1 is decoded by software to be either (1) VDP vertical sync., (2) 9901 internal timer, or (3) I/O bus generated.

9901 BIT ORGANIZATION

ADDRESS	CRU BIT	9901	PIN	FUNCTION
0000	0	Control		Control
0002	1	$\overline{INT1}$	17	External Interrupt
0004	2	$\overline{INT2}$	18	Video Display Processor Vertical Sync Interrupt
0006	3	$\overline{INT3}$	9	9901 Internal Timer Interrupt, keyboard "=" line, joystick "FIRE"
0008	4	$\overline{INT4}$	8	Keyboard "Space" line, joystick "Left"
000A	5	$\overline{INT5}$	7	Keyboard "ENTER" line, joystick "Right"
000C	6	$\overline{INT6}$	6	Keyboard "O" line, joystick "Down"
000E	7	$\overline{INT7}$ (P15)	34	Keyboard "FCTN" line, joystick "Up"
0010	8	$\overline{INT8}$ (P14)	33	Keyboard "SHIFT" line
0012	9	$\overline{INT9}$ (P13)	32	Keyboard "CTRL" line
0014	10	$\overline{INT10}$ (P12)	31	Keyboard "Z" line
0016	11	$\overline{INT11}$ (P11)	30	Not Used As Interrupt
0018	12	$\overline{INT12}$ (P10)	29	Reserved, High Level
001A-1E	13-15	$\overline{INT13}$-$\overline{INT15}$	28,27 and 23	Not Used As Interrupt

9901 I/O MAPPING

ADDRESS	CRU BIT	9901	PIN	FUNCTION
0020	16	P0	38	Reserved
0022	17	P1	37	Reserved
0024	18	P2	26	Bit 2 of Keyboard Select
0026	19	P3	22	Bit 1 of Keyboard Select
0028	20	P4	21	Bit 0 (MSB) of Keyboard Select
002A	21	P5	20	Keyboard (ALPHA LOCK)
002C	22	P6	19	Cassette Control 1 (motor control)
002E	23	P7 ($\overline{INT15}$)	23	Cassette Control 2 (motor control)
0030	24	P8 ($\overline{INT14}$)	27	Audio Gate
0032	25	P9 ($\overline{INT13}$)	28	Mag Tape Out
0034	26	P10 ($\overline{INT12}$)	29	Reserved
0036	27	P11 ($\overline{INT11}$)	30	Mag Tape Input
0038-003E	28-31	P12-P15	31-34	Not used in I/O mapping

A.6 ELECTRICAL CHARACTERISTICS

DRIVE CAPABILITY OF I/O SIGNALS

SIGNAL NAME	DRIVER
$\overline{\phi 3}$	74LS244
$\overline{CRUCLK}$	74LS244
$\overline{WE}$	74LS244
A0	74LS244
A1	74LS244
DBIN	74LS04
$\overline{MBE}$	74LS244
$\overline{MEMEN}$	74LS32
A3-A14	74LS367
D0-D7	74LS245
A15/CRUOUT	74LS244
SBE	74LS03
HOLD	74LS32
$\overline{RESET}$	74LS04

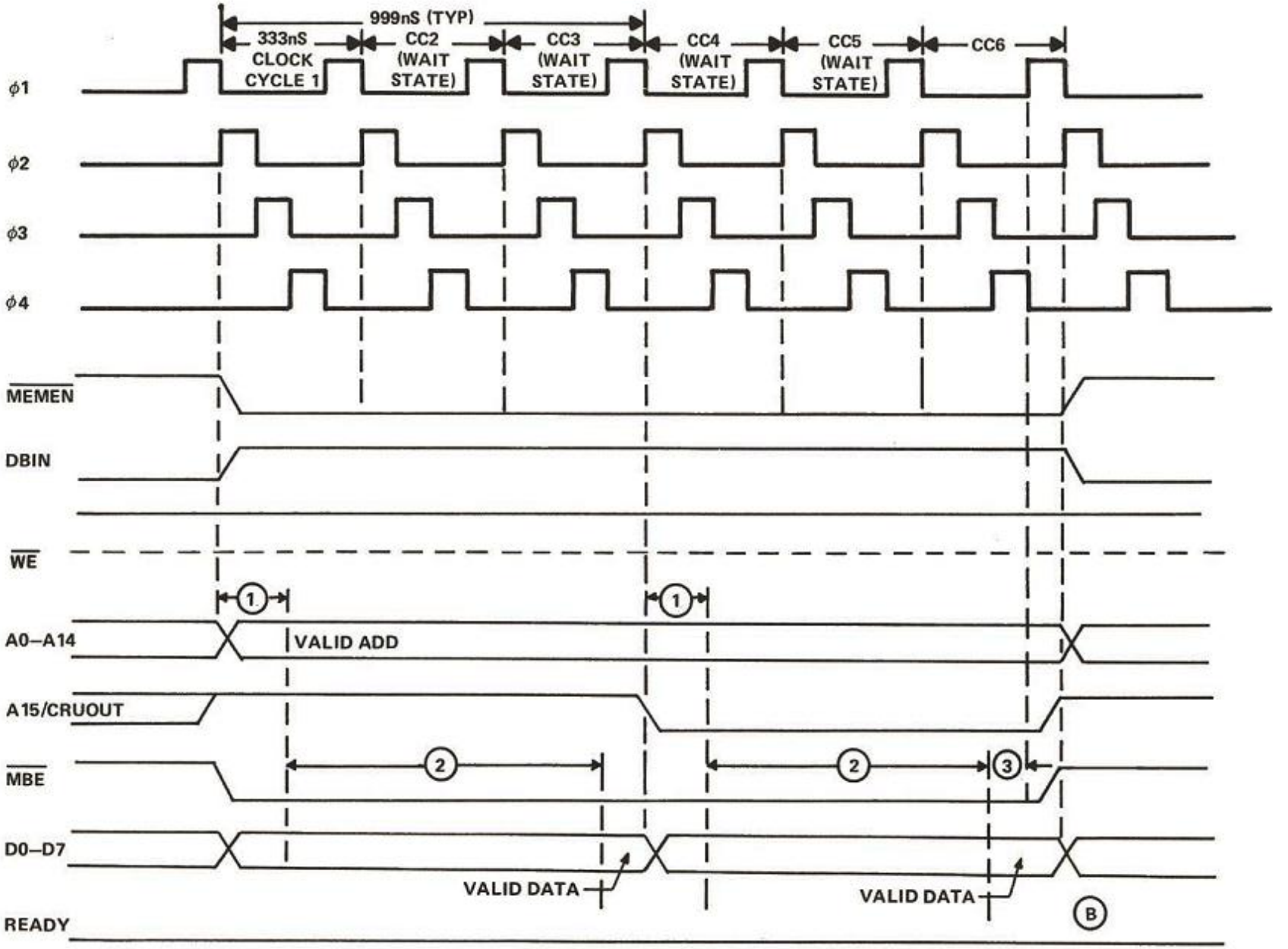
I/O READ

A CPU Read cycle for the external device consists of two 8-bit read cycles (Figure B). The two bytes read are assembled as a 16-bit word before they are presented to the 9900. Shown in Figure B are two 8-bit read cycles with one wait state inserted in each to work with slow memories.

At the beginning of clock cycle 1, $\overline{MEMEN}$ goes low true and DBIN goes high true. At the same time that $\overline{MEMEN}$ goes true, the address bus goes active. $\overline{WE}$ stays high false during the entire cycle.

In order to eliminate noise and glitches (associated with crosstalk and simultaneous switching), a minimum of 100 nanoseconds should be allowed for the address lines to settle. $\overline{MBE}$ (predecoded from A0, A1, and A2) goes true during the leading edge of $\phi 2$ of clock cycle 1. Data read from the peripherals must be valid 750 nanoseconds after the start of clock cycle 1.

The CPU will look at the full 16-bit data bus during the leading edge of $\phi 1$ of clock cycle 6. Under worst-case conditions, data must be valid 100 nanoseconds before that time.



① SETTLING TIME = 100nS (MIN)
② ACCESS TIME FOR DSR ROM + DATA Ts + DATA BUFF DELAY (PERIPHERAL + MAINFRAME) = 650nS (MAX)
③ SETUP TIME FOR 9900 = 60nS (MIN)

FIGURE B. I/O READ TIMING

I/O WRITE

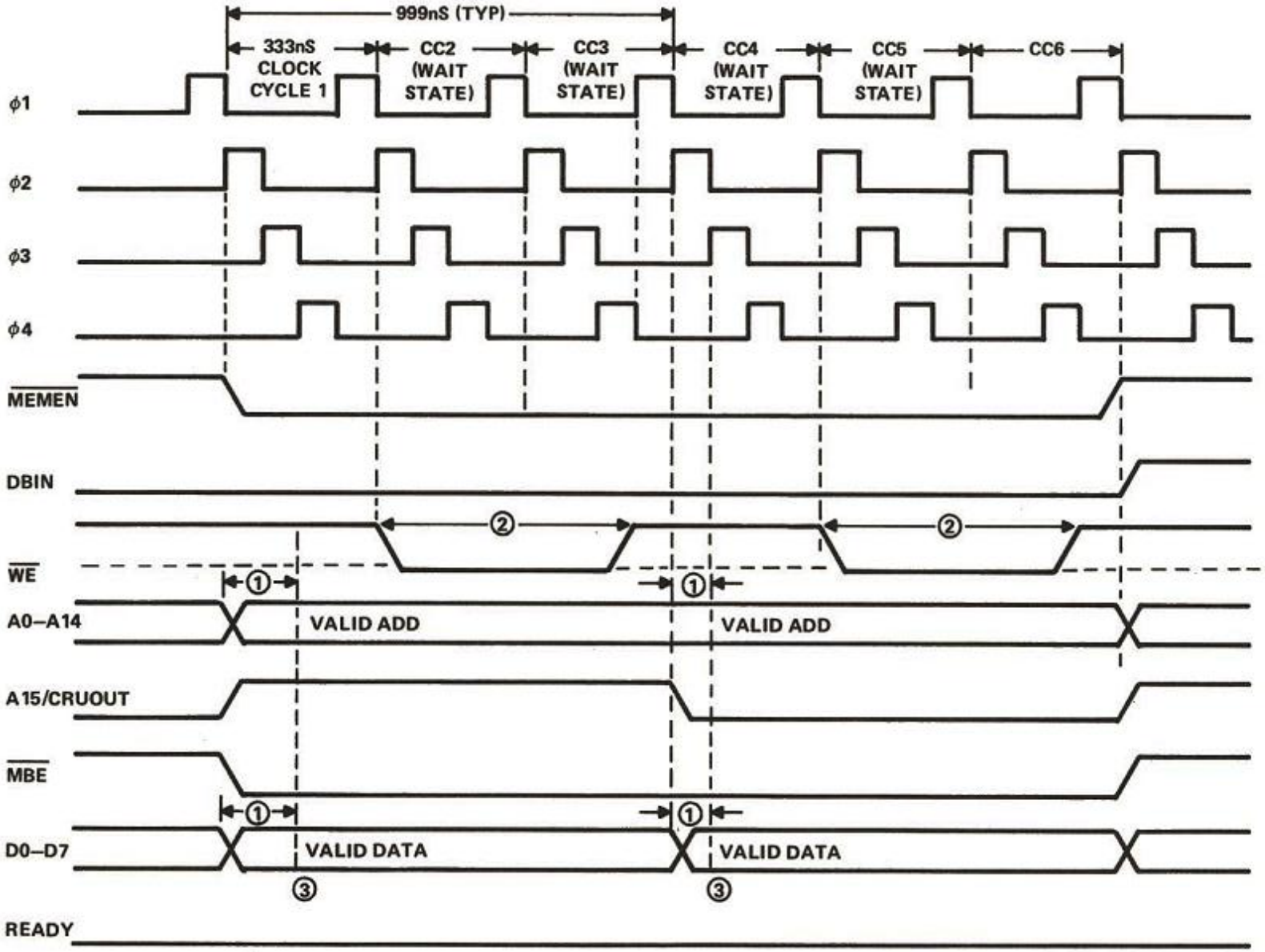
Figure C shows a 16-bit I/O write cycle. As described earlier, it is composed of two 8-bit write cycles. A write cycle will always be preceded by an ALU cycle.

$\overline{\text{MEMEN}}$ and DBIN go true (low) at the start of the cycle. A time of 100 nanoseconds (min) is allowed for the address lines to settle. $\overline{\text{WE}}$ goes true (low) on the leading edge of ϕ2 during the wait states and stays true for 666 nanoseconds (TYP).

During a Read or a Write the odd byte (LSBY) is accessed first, then the even byte (MSBY). A15/CRUOUT changes its state 1 microsecond (TYP) after the cycle is initiated. The second 8-bit write cycle is identical to the first 8-bit write. $\overline{\text{MBE}}$ stays true (low) during the entire (1.8 microseconds) cycle.

I/O BUS LOADING

SIGNAL	TOTAL SWITCHING LOAD (pF)	MAXIMUM PERIPHERAL LOAD (pF)
$\overline{\text{D0-D7}}$	210	90
A0-A2	100	90
A3-A14	100	90
A15/CRUOUT	110	100
$\overline{\text{ϕ3}}$	110	100
$\overline{\text{RESET}}$	100	90
READY	80	70
CRUIN	125	90
$\overline{\text{CRUCLK}}$	100	90
$\overline{\text{MBE}}$	100	90
$\overline{\text{WE}}$	100	90
$\overline{\text{SBE}}$	35	25
DBIN	100	90
$\overline{\text{MEMEN}}$	100	90
HOLD	80	70



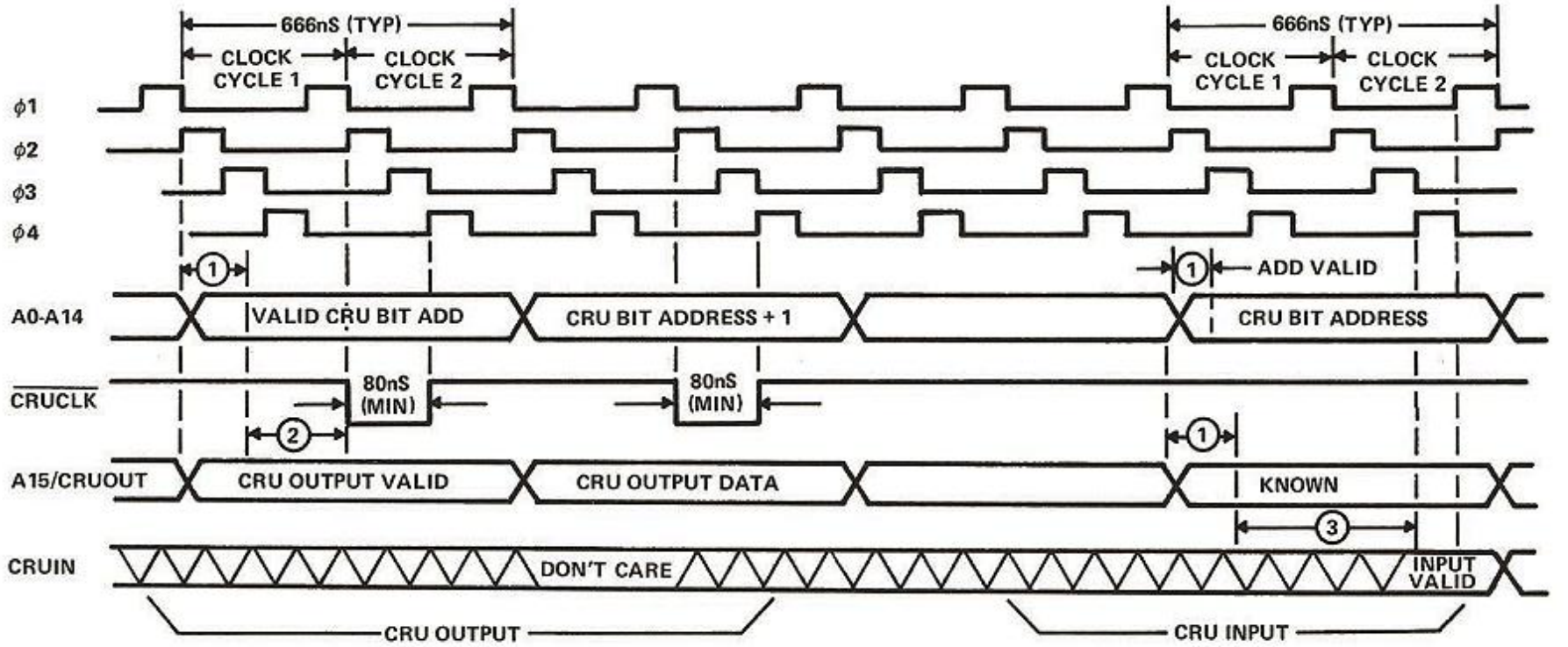
① SETTLING TIME = 100nS (MIN)
② $\overline{WE}$ PULSE WIDTH = 578nS (TYP)
③ VALID DATA

FIGURE C. I/O WRITE TIMING

CRU TIMING

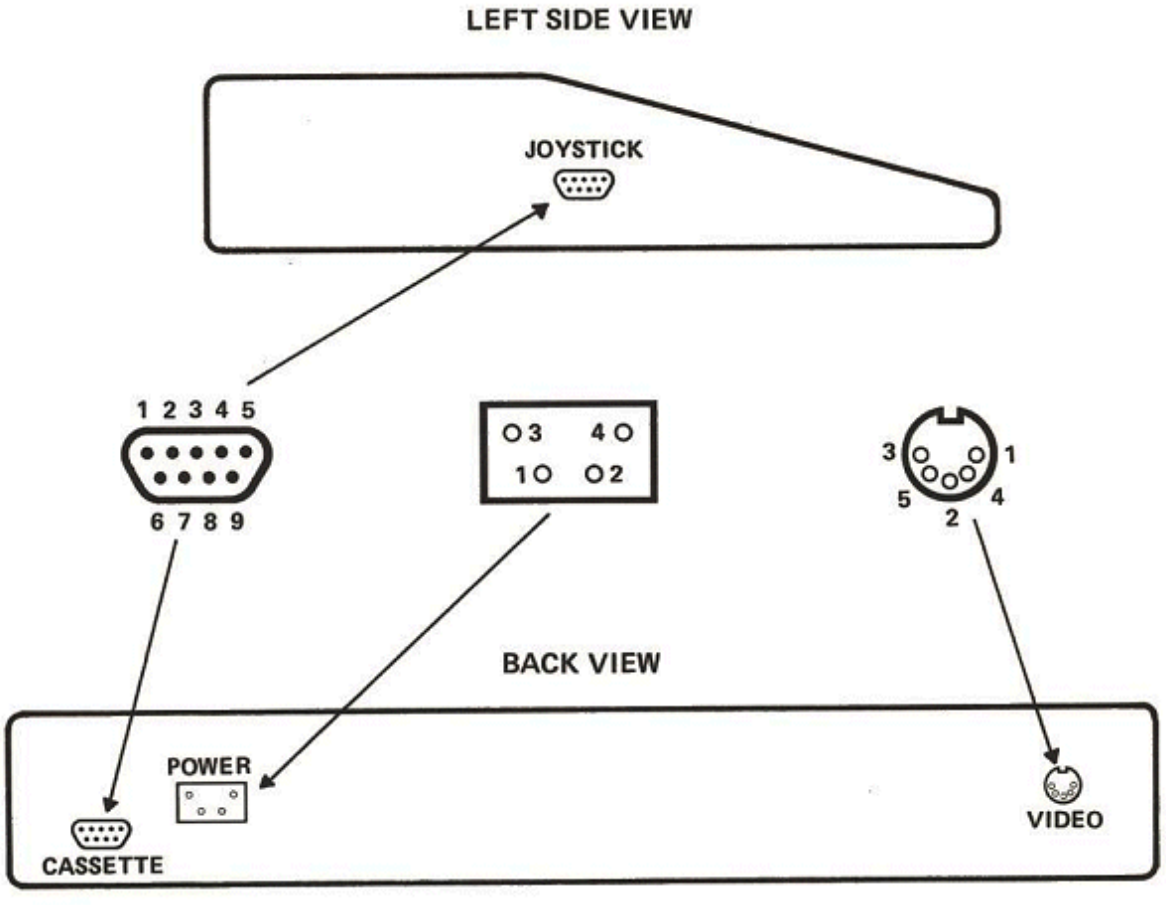
CRU interface timing is shown in Figure D. The CRUOUT cycle is composed of two clock cycles. When placed on the address bus A0 through A14, the CRU bit address is allowed to settle for 100 nanoseconds (min). CRUCLK is a 63 nanoseconds (max) low true signal which occurs on the trailing edge of ϕ1 of clock cycle 2. CRUOUT data is valid at the start of clock cycle 1 and is latched by the CRUCLK in the respective peripheral.

CRUIN also consists of two clock cycles of 666 nanoseconds (TYP). Again 100 nanoseconds is allowed for the address bus to settle. The CPU samples the CRUIN line on the leading edge of ϕ1 of clock cycle 2. Data must be valid 40 nanoseconds (min) before that. This implies an access time of less than 400 nanoseconds for CRUIN.



① SETTLING TIME = 100nS (MIN)
② ADD VALID TO $\overline{\text{CRUCLK}}$ = 233nS (TYP)
③ ADD VALID TO VALID CRUIN = 400nS (MAX)

FIGURE D. CRU TIMING



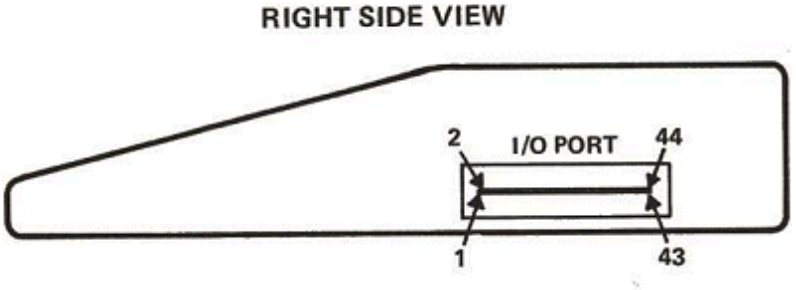


FIGURE E. CONNECTOR PIN IDENTIFICATION DIAGRAM

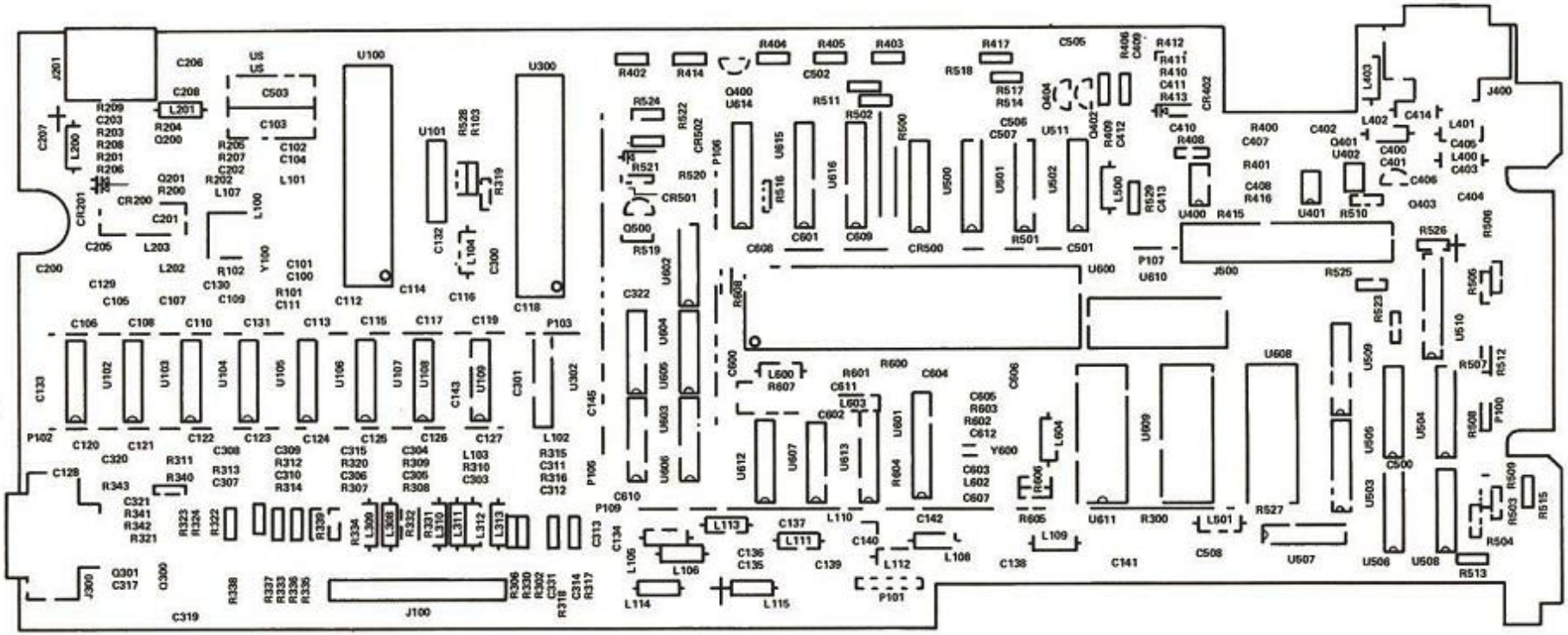


FIGURE F. TI-99/4A LOGIC BOARD COMPONENT LOCATION DIAGRAM

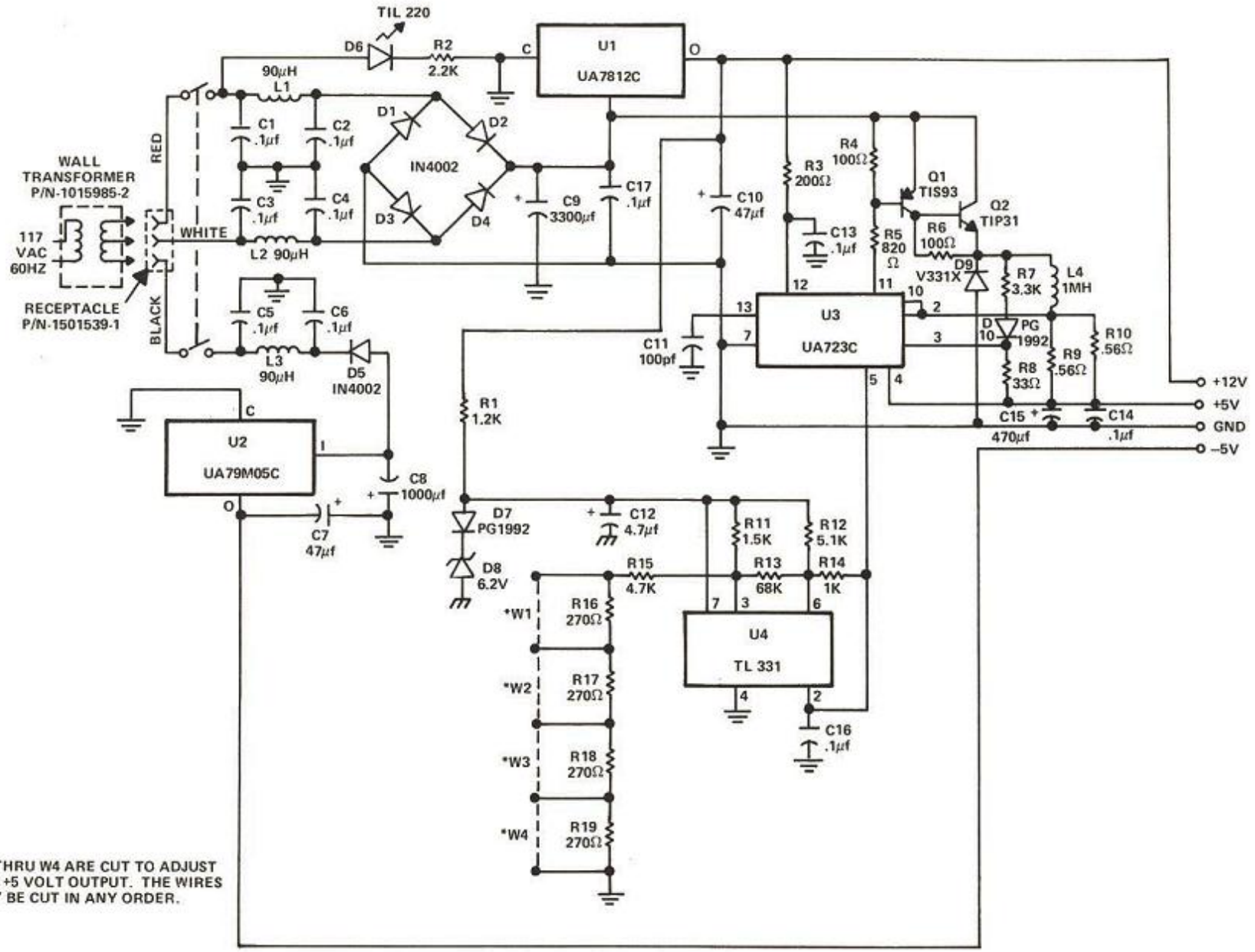


FIGURE G. TI-99/4A CONSOLE POWER SUPPLY

GLOSSARY

ALU	Arithmetic Logic Unit.
bit	Smallest unit of memory; BInary digiT.
byte	8 bits of memory.
cartridge memory	ROM space found within a plug-in cartridge.
CPU	Central Processing Unit.
CRU	Communication Register Unit (I/O techique for TMS 9900 Microprocessor).
DRAM	Dynamic Random Access Memory.
GPL	Graphics Programming Language.
GROM	Graphics Read-Only Memory (TMC 0430). This memory device is a 6144 byte read-only memory with on-board 13-bit program counter. The program counter can be written or read through an 8-bit interface and will automatically increment.
I/O	Input/Output.
LSB	Least Significant Bit.
LSBY	Least Significant Byte.
MMD	Memory-Mapped Device.
MSB	Most Significant Bit.
MSBY	Most Significant Byte.
MPU	Microprocessor Unit.
PC	Program Counter.
PCB	Printed Circuit Board.
RAM	Random Access Memory.
ROM	Read-Only Memory.
SRAM	Static Random Access Memory.
VDP	Video Display Processor (TMS 9918A).
WORD	16 bits/2 bytes of memory.

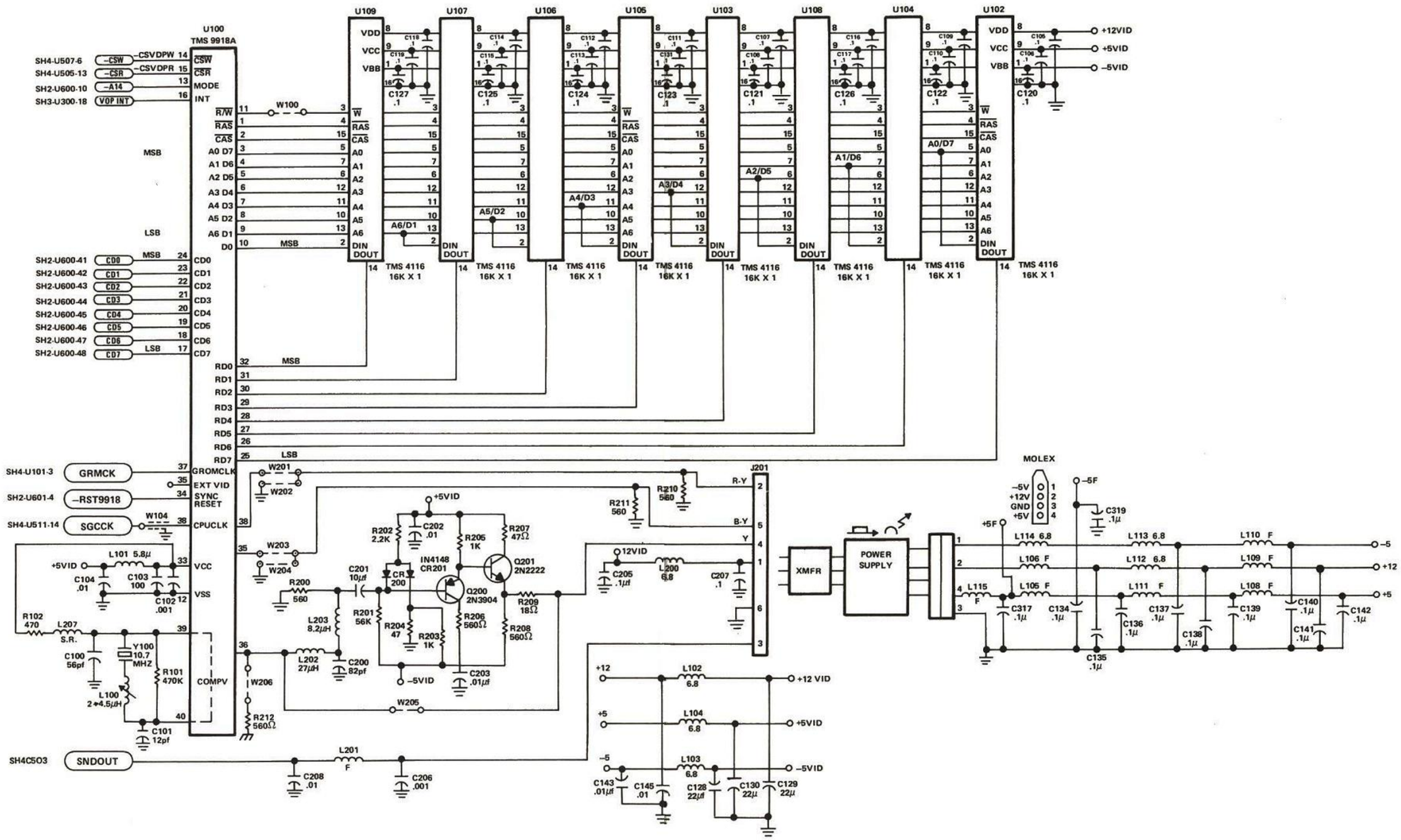
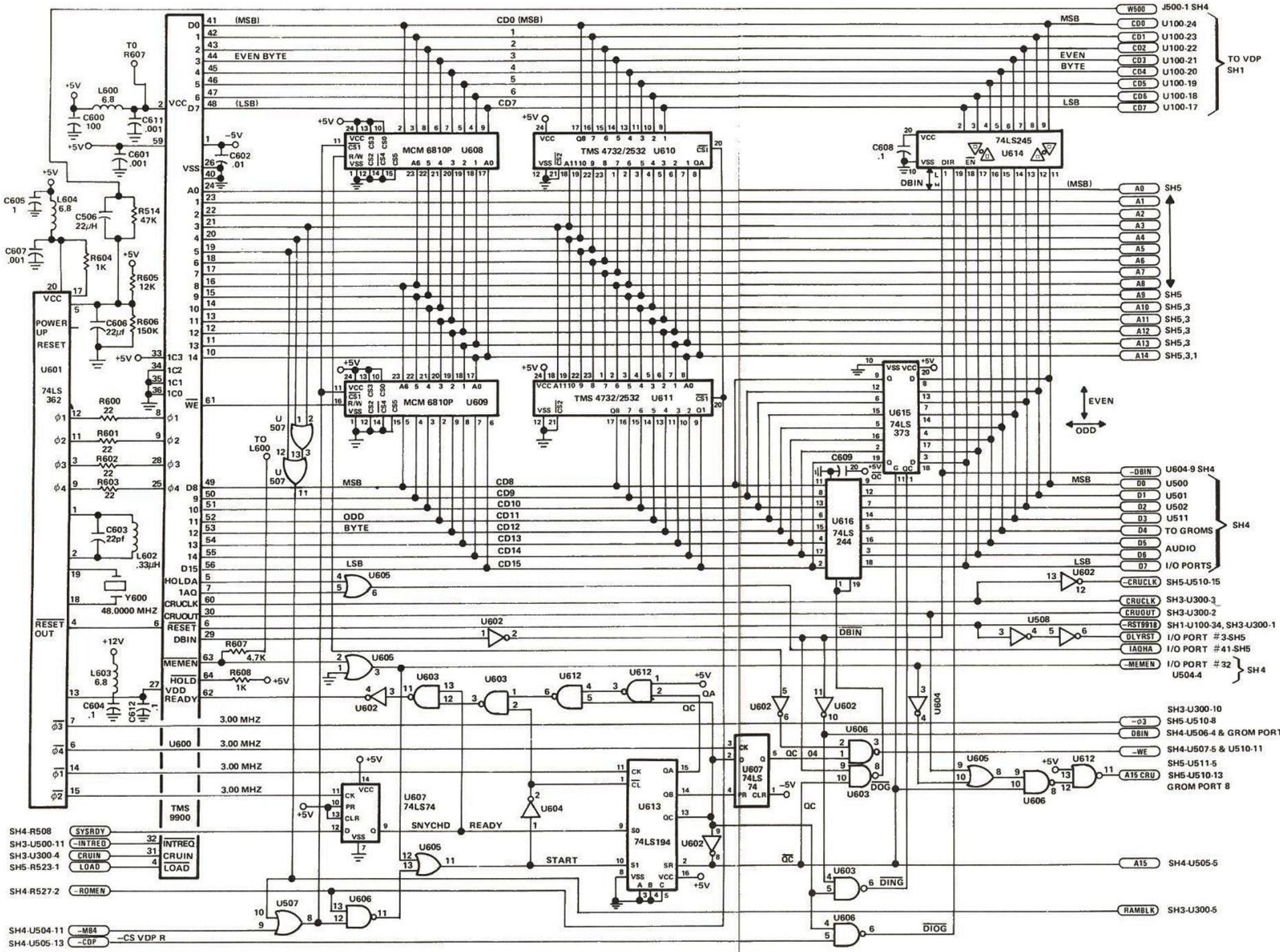


FIGURE H. TI-99/4A SCHEMATIC DIAGRAM



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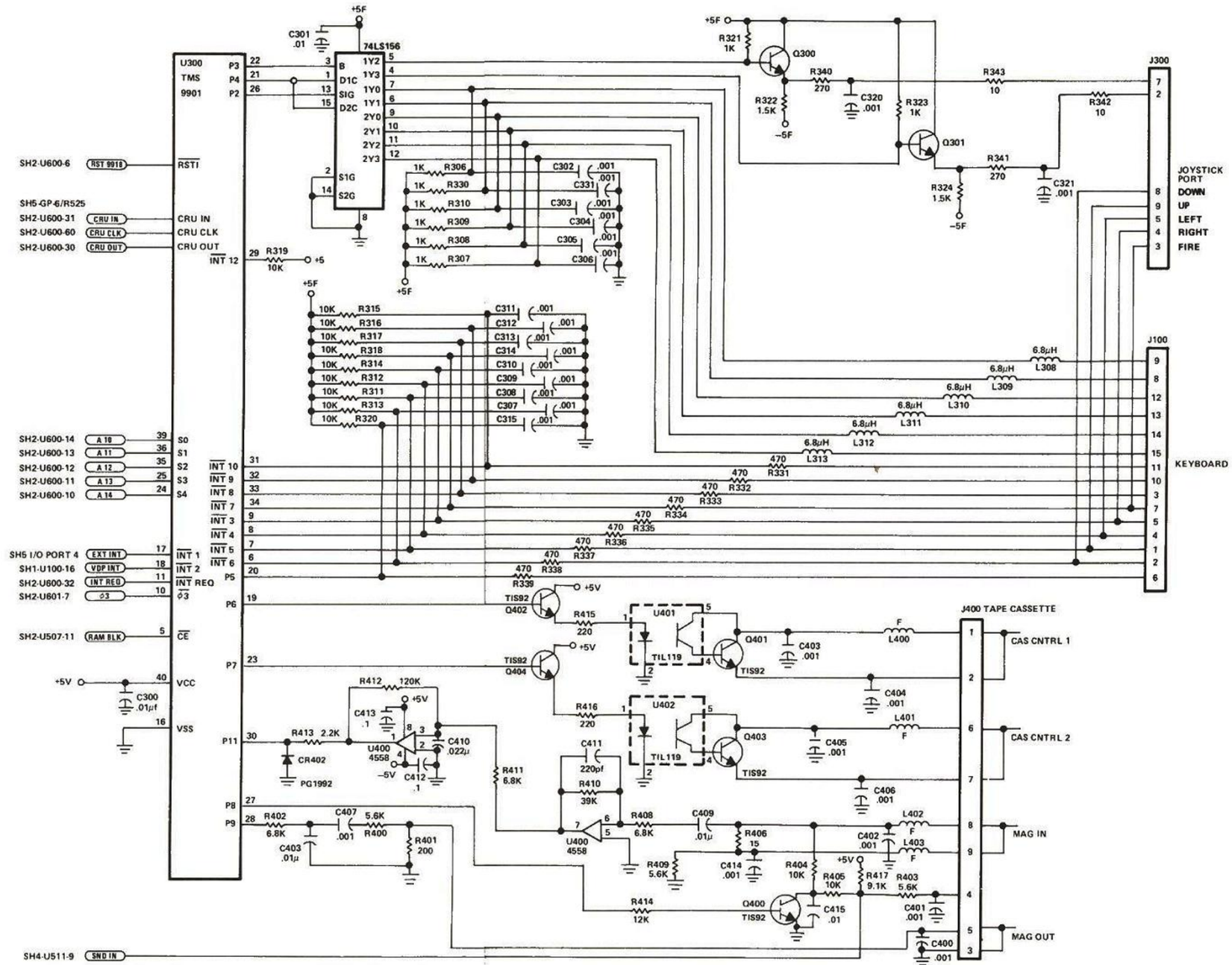

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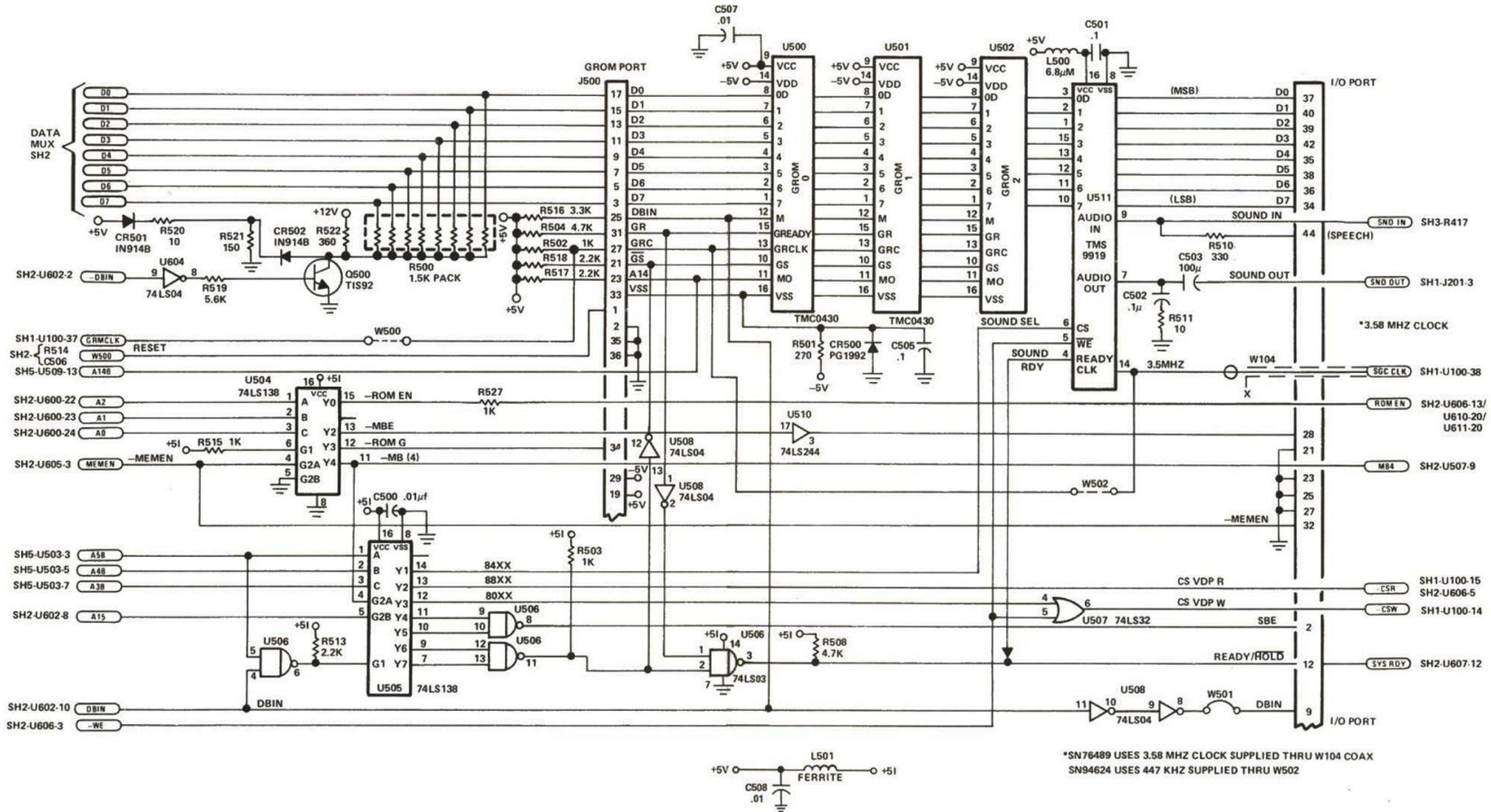

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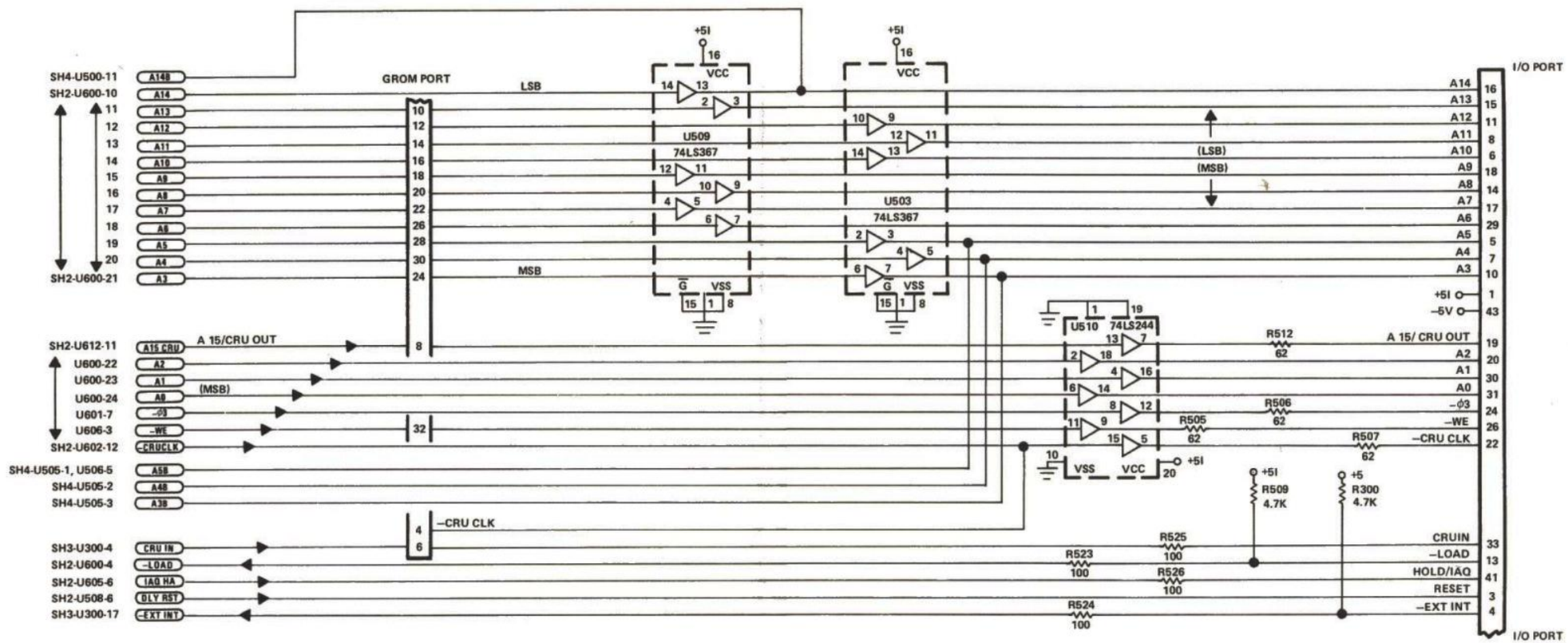

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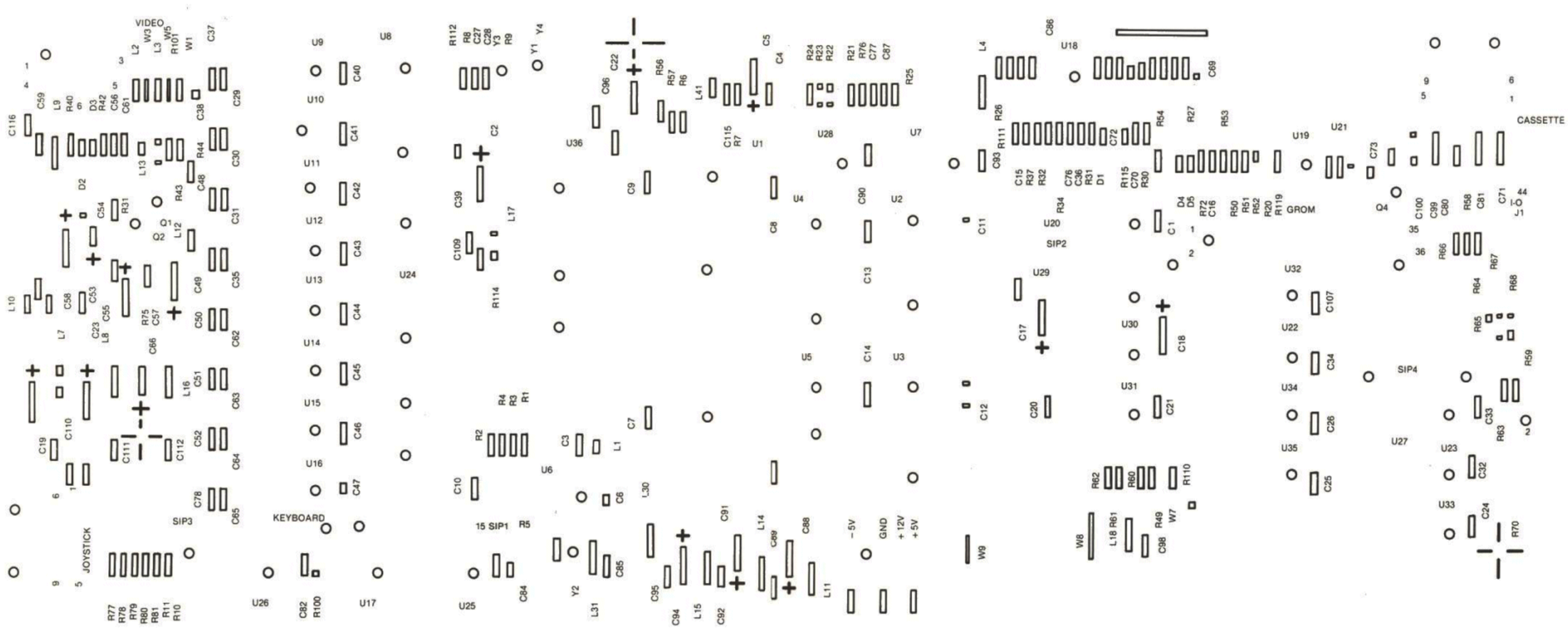
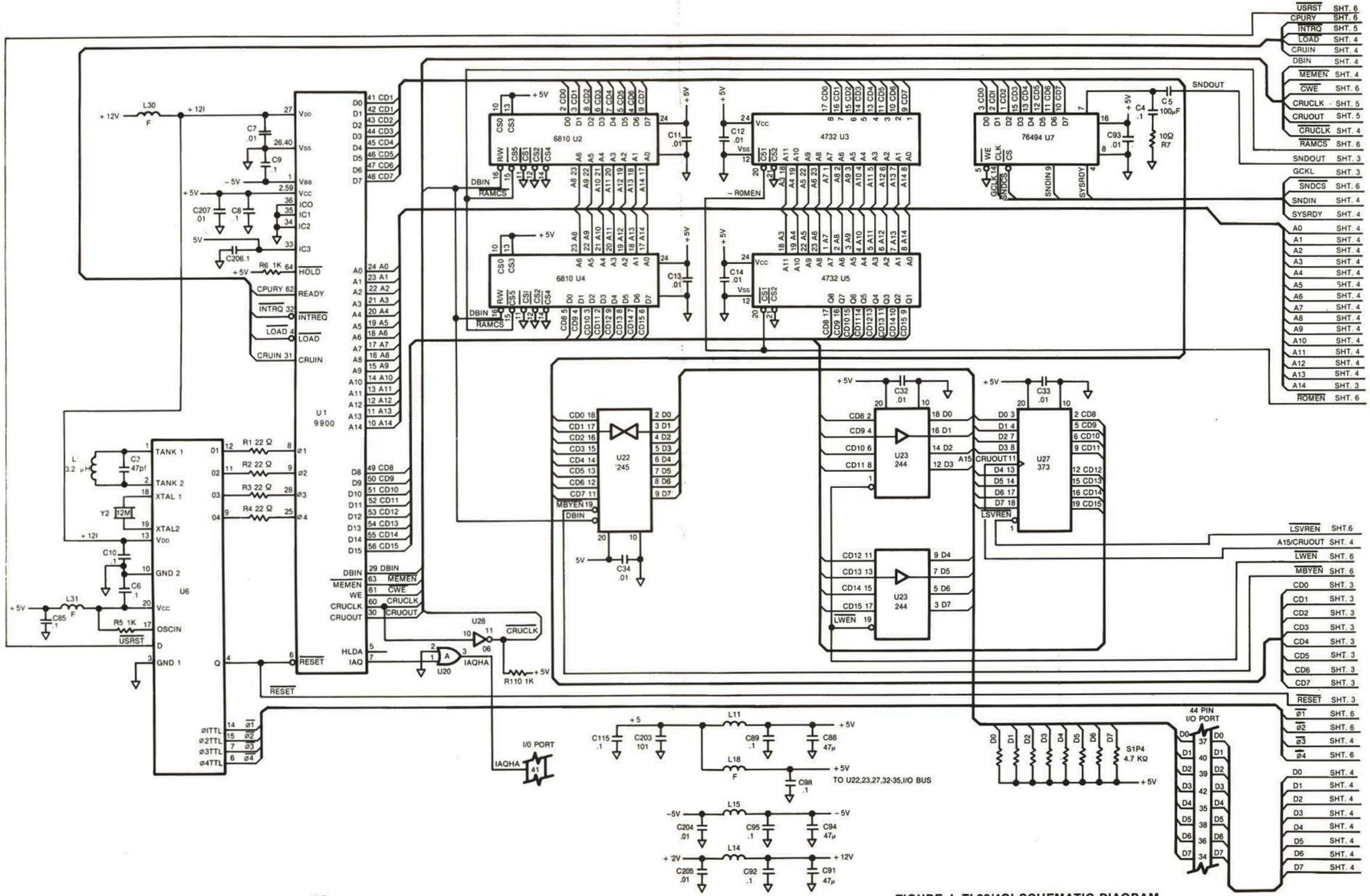


FIGURE I. TI-99/4QI LOGIC BOARD COMPONENT LOCATION DIAGRAM



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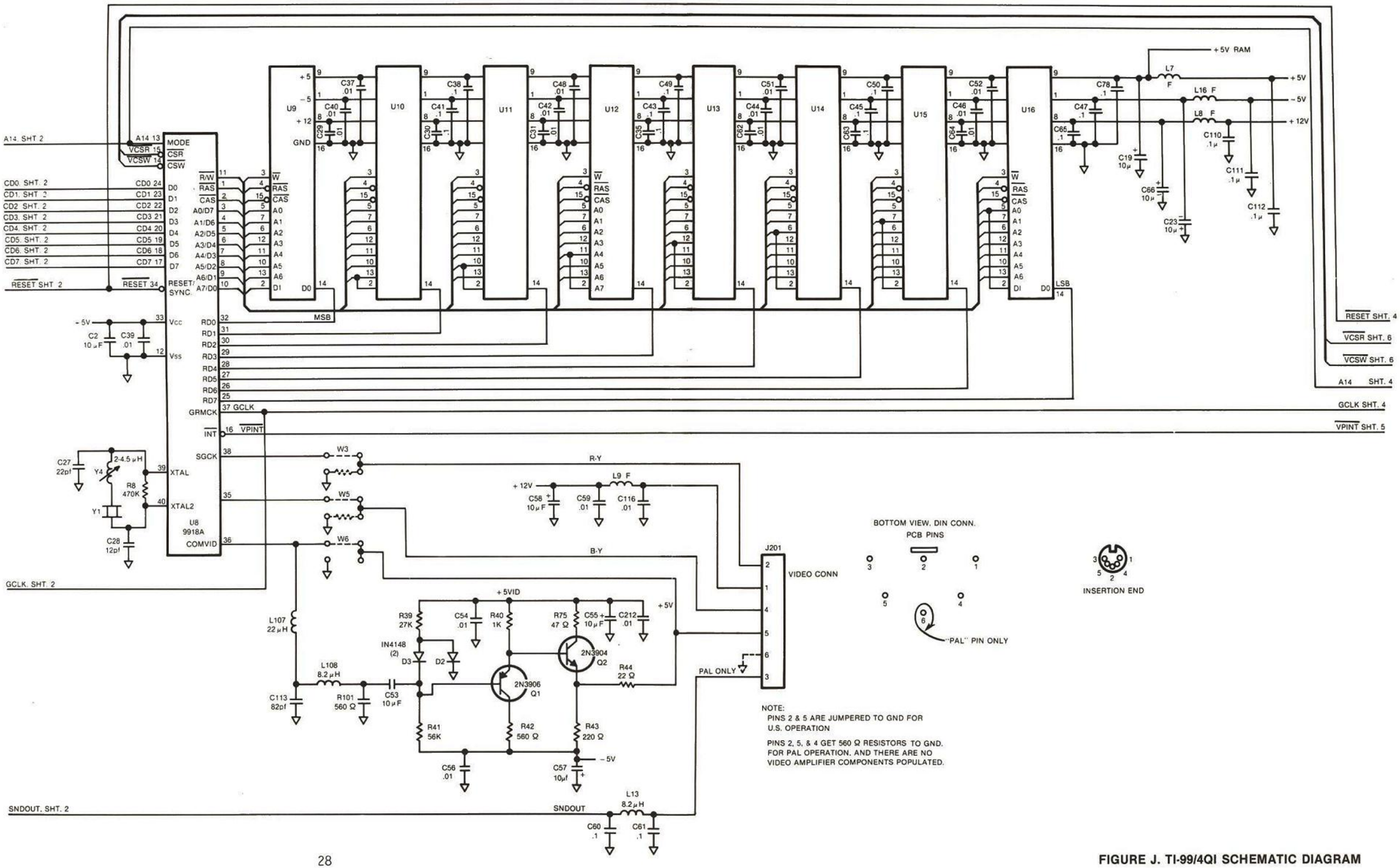

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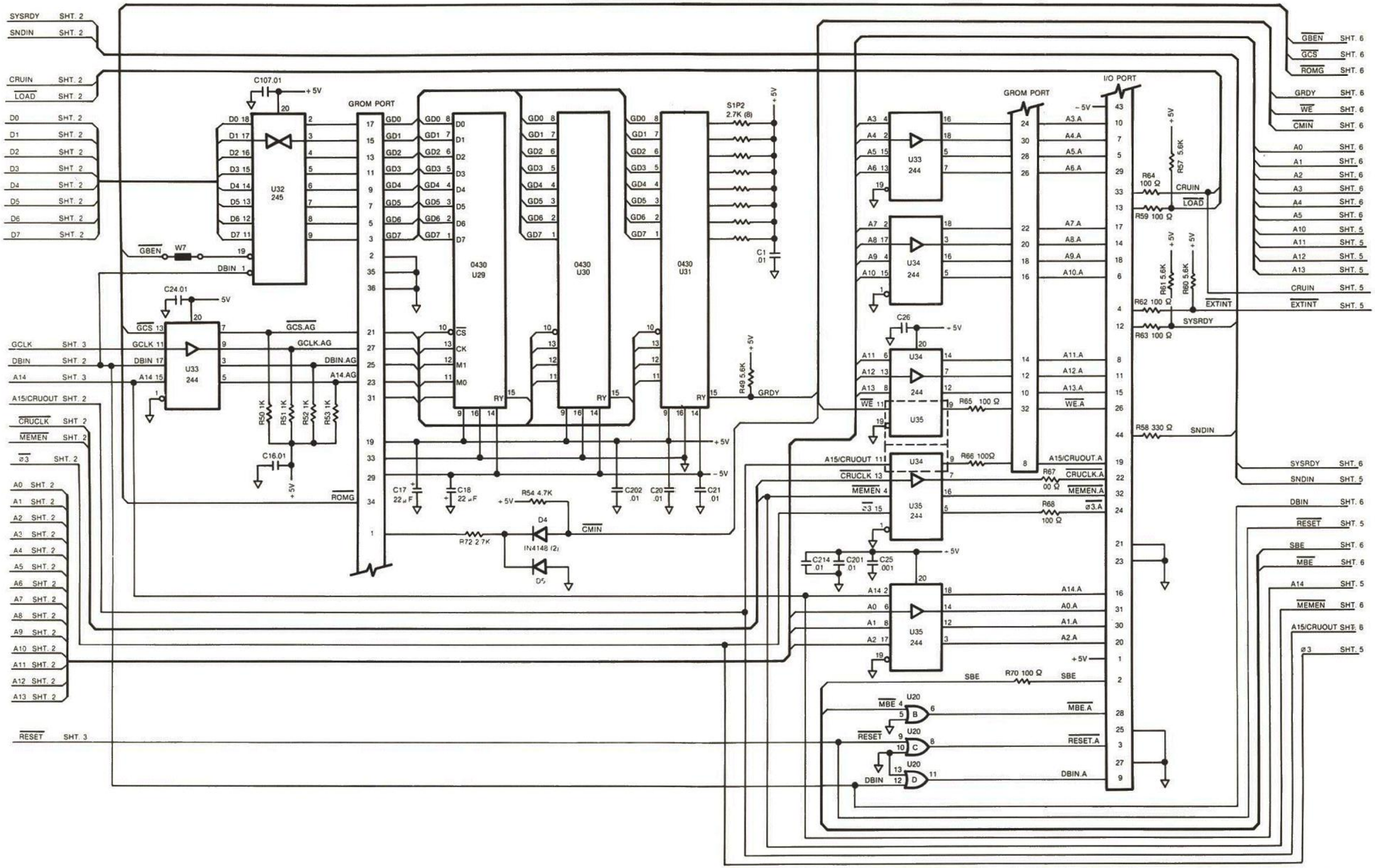

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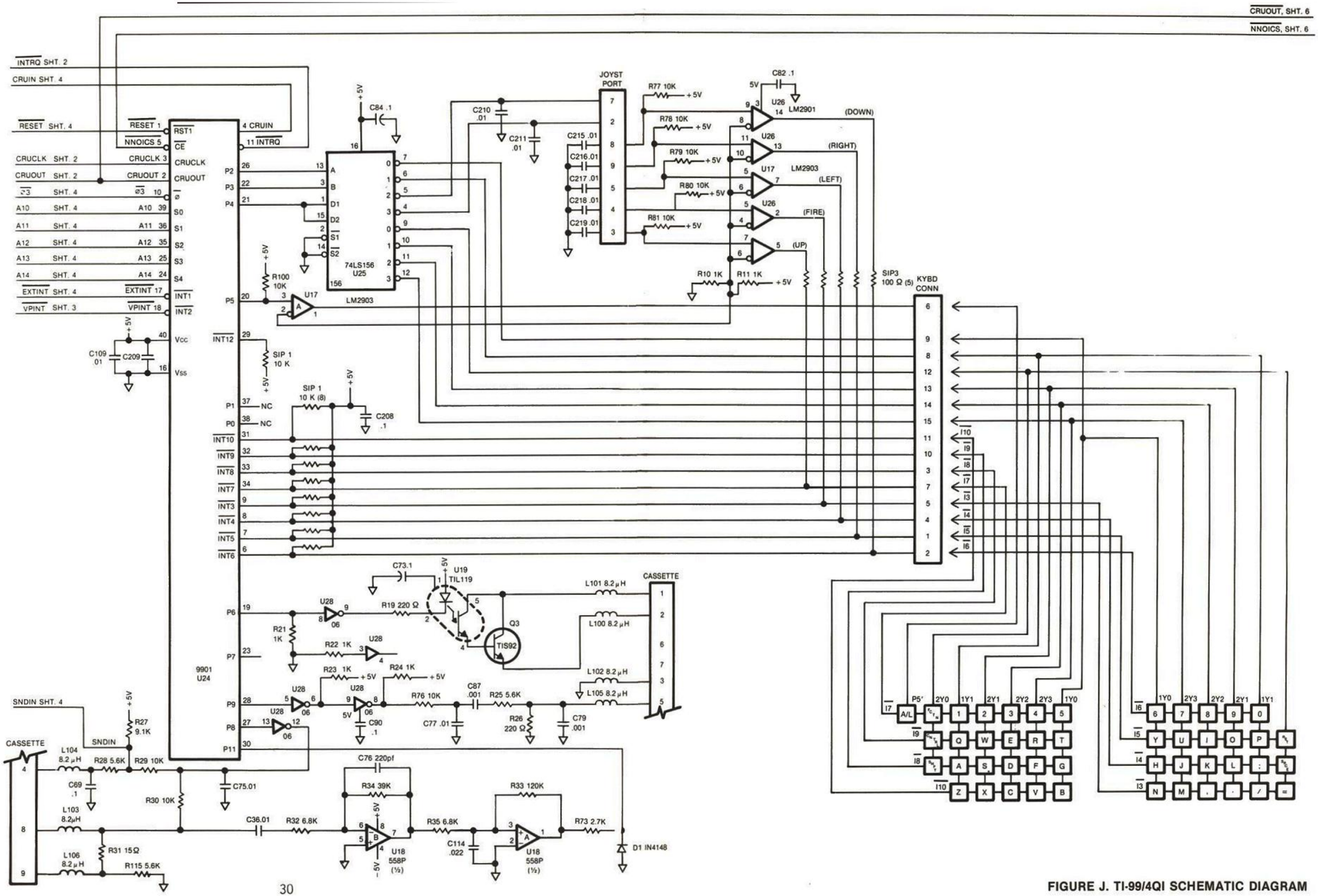

FIGURE J. TI-99/4QI SCHEMATIC DIAGRAM

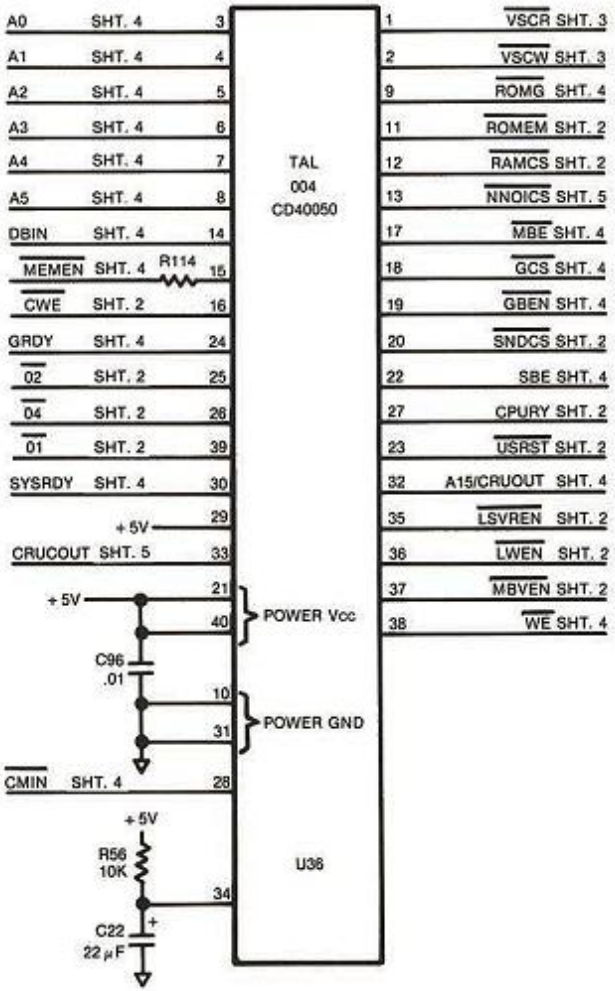

FIGURE J. TI-99/4QI SCHEMATIC DIAGRAM